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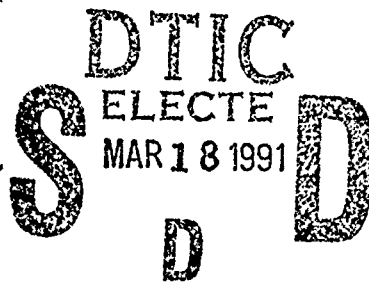


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# QUALIFICATION PROCEDURES FOR VHSIC/VLSI

GE Aerospace

Thomas A. Baumes



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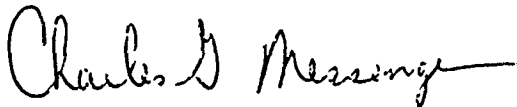
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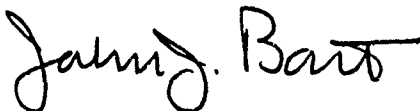
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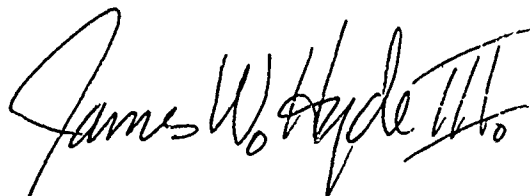
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13. ABSTRACT (Maximum 200 words)  This program developed, outlined, refined and verified the test methodology and qualification criteria and procedures to be used to ensure the integrity and reliability of microcircuit devices designed for insertion into military systems. A major portion of the criteria and procedures, reflected herein, enables a significant reduction in time and cost of the microcircuit Quality/Reliability Assurance process by addressing up front simulations during design prior to commitment, complex and expensive manufacturing processes with in-line quality processes controlled by a SPC (Statistical Process Control) program and ongoing QA Program using their TRB (Technology Review Board) and SEC (Standard Evaluation Circuit) programs.				
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## EVALUATION

This program was sponsored by the VHSIC program office to investigate and develop an alternative approach for qualification of complex microcircuits. To address the technical issues related to a process oriented qualification approach, the contractor organized an Industry Coordinating Working Group (ICWG) which was divided into four microcircuit manufacturing disciplines: design, fabrication, assembly, and test. The ICWG spawned and refined several key concepts, such as Technology Review Board (TRB), Technology Characterization Vehicle (TCV) and Standard Evaluation Circuit (SEC). These concepts were then integrated with Total Quality Management (TQM) principles and formulated the basis for the Qualified Manufacturer's List (QML).

The final output of the program was a DOD specification MIL-I-38535, "General Specification for Integrated Circuit Manufacturing." This document details the requirements a manufacturer must address in order to be listed on the QML. Presently, several refinements to the requirements are ongoing. These refinements are addressing issues related to radiation hardness and third party design. Overall, this program was very successful and provided the DOD with an approach to qualifying high complexity Application Specific Integrated Circuits (ASIC) for system usage.

  
CHARLES G. MESSENGER

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Appendix B	Proposed Test Methods for VHSIC/VLSI Generic Qualification
Appendix C	Proposed Requirements to Qualify CAD Tools for VHSIC/VLSI Devices

## 1. INTRODUCTION

### 1.1. GENERAL

In September of 1986, GE/AES, Utica, NY received a contract to develop a Generic Qualification approach to microcircuit qualification that would not only benefit the military acquisition arena but also develop a methodology of microcircuit process control to promote the United States to a position of supplying the highest quality and most reliable microcircuits in the world. This contract was awarded and administered by RADC.

In order to expand the technical team and provide expertise in the areas of commercial and bi-polar techniques and technologies, two subcontracts were awarded by GE to AT&T Bell Lab, Allentown PA and Honeywell Inc, Plymouth MN.

This effort was performed in conjunction with the VHSIC Program and the DOD effort to streamline the acquisition and costs of microcircuits used by the DOD. The Industry Coordinating Working Group (ICWG) which included the Government, Industry and Academia was formed to provide technical insights, critiques, and guidance in support of this effort.

### 1.2. PROGRAM OBJECTIVE

This program was derived to develop a new approach to qualifying complex microcircuits. Recent trends in military systems showed that there was wider use of low volume, complex, application specific integrated circuits and less reliance on high volume standard microcircuits. As a result there was an explosive increase of nonstandard, noncertified and nonqualified microcircuits in new systems. This raised concerns over system logistic support, reliability and availability.

Also studies of the DOD VHSIC program suggested that it was no longer economical to qualify piece parts using existing qualification procedures, due to the cost, complexity and relatively low quantity production of individual VHSIC/VLSI device designs. The advent of Computer Aided Design (CAD) tools which accurately simulate and predict device performance before

actual production allowed for more efficient and economical means of production and testing thus allowing quality and reliability to be designed in instead of tested in.

These issues along with the inability of the existing qualified parts list (QPL) system to handle these new device trends were the impetus for this program.

The objective, then, of this program was to develop a new approach to microcircuit qualification based on process control while taking advantage of new tools, such as Statistical Process Control (SPC) and CAD, and assure the quality and reliability for use in military systems of those devices produced from that process. All aspects related to microcircuit manufacturing from design through final test were to be addressed in the new procedures.

Three tasks were defined to accomplish this objective:

- o Task I - Review and Definition - review existing procedures for applicability to VHSIC/VLSI devices.
- o Task II - Investigation - research technical issues through the establishment of an Industry Coordinating Working Group (ICWG) and propose new procedures.
- o Task III - Verification and Demonstration - verify and demonstrate the new procedures on the contractors' manufacturing process. Make improvements to the procedures based on the outcome of the demonstration.

### 1.3. SUMMARY OF RESULTS

The Qualification Procedures for VHSCI/VLSI program resulted in the following major accomplishments:

Existing military documents associated with microcircuit qualification were reviewed for applicability. This review outlined several areas where changes were necessary to facilitate the qualification of complex VHSIC/VLSI

devices in military systems. To better address these issues and develop technical approaches, an Industry Coordinating Working Group (ICWG) was established. The ICWG recommended a quality management oriented approach to the problem. The contract team of GE, AT&T and Honeywell utilized many of the proposed recommendations of the ICWG in formulating a draft procedure.

Finally, a qualification procedure document was developed, completed and issued (on 18 Dec 1989) as MIL-I-38535, "INTEGRATED CIRCUIT MANUFACTURING, GENERAL SPECIFICATION FOR" (see Appendix-A). The MIL-I-38535 document establishes the general procedures and the quality and reliability assurance requirements for the manufacturing and acquisition of integrated circuits. Key to quality and reliability assurance is the requirement for quality management. Through quality management, a manufacturer is positioned to provide to the marketplace a cost effective, high quality and reliable microcircuit within the DoD acquisition requirements, as well as the commercial requirements, as a qualified manufacturer. Also, the DoD is ensured of the best possible integrated circuits qualified and ready for insertion in shorter cycle times.

Alpha site demonstrations were performed by GE and AT&T to provide confirmation of the applicability of the new procedures. Based on the results, changes to the QML requirements were recommended and implemented in MIL-I-38535. Following Alpha site demonstrations, Beta site meetings were held to further enhance the requirements applicability and acceptance.

Other outputs of this program included draft versions of new test methods for testing digital microcircuits. Also, a Manufacturing Guidelines document was developed to provide an up-to-date index of tools which can be utilized to improve manufacturing quality.

The particulars of these tasks are discussed in more detail in the following sections.

## 2. TASK I - REVIEW OF DOCUMENTS

### 2.1. OBJECTIVES

The objective of the review of existing MIL-STD documents was to use the teams' awareness of existing procedures and methods to determine which of the existing military documents require attention for implementation of the new qualification approach for VHSIC/VLSI. The approach encouraged utilization of that which is still relevant; identify areas that needed new methods or procedures; and flag areas not presently covered.

The review of the documents categorized them into one of the following:

- o Retain: when the document was relevant to VHSIC/VLSI and needs no modification.
- o Modify: when the document was generally useful but requires modification for VHSIC/VLSI application, or because it required more clarity in the definition of the procedures, or for improved readability and/or user-friendliness.
- o New: when the objectives of the document remained valid but new methods are needed for VHSIC/VLSI applicability.
- o Not applicable: when the scope of the document was not pertinent to VHSIC/VLSI.

In addition to determining the usefulness of existing documentation, the team sought to identify gaps. Today's qualification approach is heavily dependent on testing of finished product, whereas the new approach seeks to qualify the processes that yield the finished product. It was, therefore, necessary to identify areas not covered by today's methods which will need to be covered under the new approach. For example, the process by which ICs are designed is minimally covered under existing procedures, but it will be critical under the new approach to identify a method for assuring that design rules are adhered to, and that CAD tools are adequate. Some new approaches to qualification were considered by the team at the beginning of Task 1, such

as "Parametric Monitors" (PMs) for checking the electrical performance parameters of a process and "Standard Evaluation Circuits" (SECs) which can be used in place of the actual circuits for many of the require reliability tests.

## 2.2. APPROACH

The approach taken by the Task 1 team to best meet the objectives was:

- o Establish a basis for the review criteria to give commonality in evaluation procedures.
- o Assign document review responsibility on basis of expertise and available resources.
- o Coordinate document reviews with weekly and monthly status reviews on progress.
- o Summarize results and collate into four basic categories. (Not Applicable-N/A, Modify-Mod, Modify to include surrogate-Mod\*, and Retain-Ret)
- o Include plans for ICWG involvement in document review through ICWG structuring and recruiting.

A common review sheet was prepared and distributed. The review sheet contained three main sections providing:

- o A description of what was being evaluated.
- o What reliability information was gained.
- o Will modification be required for VHSIC?

With each document assigned for review, subtest methods and/or subparagraphs were partitioned and reviewed by assigned personnel.



To monitor progress and allow for continual interaction of all functions, weekly and monthly status reviews were held. This ensured that individual document reviewers were cognizant of concerns and accomplishments of the entire Task 1 team.

The review sheets were then summarized and collated to provide categorization for Task 2 follow-up review by the ICWG.

## 2.3. RESULTS

### 2.3.1. MIL-M-38510F: General Specification for Microcircuits

#### 2.3.1.1. Discussion of MIL-M-38510F

The review of this document identified areas that were not compatible and/or adequate to VHSIC/VLSI technology. These are detailed below:

Paragraph 3.5 - Design and Construction: This section provides guidelines to be implemented in design. The major comment for this section is that it does not address CAD issues. Certification and monitoring of CAD is key to the new approach.

Paragraph 4.4.2 - Qualification (per MIL-STD-883C, Method 5005); and Paragraph 4.5 - Quality Conformance inspection (per MIL-STD-883C, Method 5005): this document requires that Method 5005 be used on real product, which implies high cost for low volume product such as VHSIC. In its present form, no provision is made for the use of PMs and SECs. The new approach will emphasize the use of PMs and SECs as a way to certify and monitor the processes that yield the final product.

Paragraph 4.6 - Screening (per MIL-STD-883C, Method 5004): the document requires testing of 100% of product per all the applicable tests in Method 5004. Some of the screening procedures are not effective for VHSIC/VLSI application. One example is the Method 2010, Internal Visual, which has very limited application to devices with very small design features.

Appendix A - Product Assurance Program: this appendix addresses documentation, certification, qualification and other aspects of the product realization flow, from design to outgoing inventory. Many of the issues cited from the main body of the MIL-M-38510 document, apply here as well. For example, Paragraph 20.1.1.6 - Design, Processing, Manufacturing, Equipment, and Materials Instructions, does not address CAD, PMs, or SECs.

2.3.1.2. Major Findings in MIL-M-38510F

The major findings of this review of MIL-M-38510F are:

- o Modification of the document is required for VHSIC/VLSI application.
- o CAD is not addressed.
- o Some of the screening procedures are not suitable for VHSIC/VLSI (e.g., High Power Visual Inspection).
- o Qualification and Quality Control Inspection procedures need to be modified for VHSIC/VLSI application because: the procedures are product, not process, oriented; no use is made of PMs or SECs; and sampling plans assume high volume production.
- o The document is complex, which makes it hard to follow, and prone to misinterpretation.

### 2.3.2. MIL-STD-883C

#### 2.3.2.1. Discussion of Series 1000 and 2000 Methods

The Tables 1 and 2 below list the results of the review. The column labeled "VHSIC QRA Disposition" reflects the reviewer's current thinking on the applicability of the method to the new VHSIC QRA approach. The "Comments" column captures the underlying reasons for the disposition. The column labeled "Additional Comments for Task 2" provides recommendations and/or raises flags for the team to address during the Task 2 activity. The footnote reference to "surrogate devices" alludes to tests being performed on Process Monitors (PMs) or Standard Evaluation Circuits (SEC) rather than the primary product.

#### 2.3.2.2. Major Findings in 1000 and 2000 Series

- o Most of the test methods in the 1000 and 2000 series remain applicable, either "as is" or with modification. Some test methods may need to be developed to properly address the QML approach. In some cases, it is envisioned that the QML approach may call for tests to be performed in a step of the product realization chain replacing tests that are now performed elsewhere downstream in the manufacturing cycle.
- o Many Test Methods may require updating for:
  - Use with PMs and SECs;
  - Application to VHSIC/VLSI technology requirements;
  - Clarification of test criteria, purpose, assumptions, and technical references, where possible.

TABLE 1. ANALYSIS OF MIL-STD-883C: TM 1000 SERIES

Method No.	Environmental Tests	VHSIC QRA Disposition	Comments	Additional Comments of Task 2
1001	Barometric Pressure	NA		-
1002	Immersion	NA		-
1003	Insulation Resistance	Mod*	Insufficient Voltage Range	Assembly: Address during package design.
1004	Moisture Resistance	Mod*	Needs Clarity	Address in SQC/QRA**:relate to device application
1005	Steady State Life	Mod*	Needs Clarity	Address in SQC/QRA**:relate to device application
1006	Intermittent Life	Mod*	Similar to 1005; Needs Clarity	Address in SQC/QRA**:relate to device application
1007	Agree Life	Mod*	Similar to 1005; Needs Clarity	Address in SQC/QRA**:relate to device application
1008	Stabilization Bake	Ret	Review Procedures	-
1009	Salt Atmosphere (Corrosion)	Mod		Address in SQC/QRA**:relate to device application
1010	Temperature Cycling	Ret		-
1011	Thermal Shock	Mod*	Larger Packages	-
1012	Thermal Characteristics	Mod*	Larger Chips/Packages	-
1013	Dew Point	Ret*		Address in Assembly: new techniques?
1014	Seal	Ret		SQC/QRA**: Address infant mortality
1015	Burn-In Test	Mod*	Dynamic Burn-In Difficult	-
1016	Life Reliability	Mod*	Review Test Conditions/Procedures	-
1017	Characterization	Mod*	Simulation Correlation	Address in Design/Electrical Test
1018	Neutron Irradiation	Mod*	Questionable	Address in Assembly
1019	Internal Water Vapor Content	Mod*	Poor Reproducibility	Address in Design/EI Tests, Relate to application.
1020	Steady State Total Dose	New*	Consider New Techniques	Address in Design/EI Tests, Relate to application.
1021	Irradiation	Mod*	Simulation Correlation	Address in Design/EI Tests, Relate to application.
1022	Radiation Induced Latch Up	Mod*	Simulation Correlation	-
1023	Dose Rate Threshold for Upset of Digital Microcircuits	N/A		-
1024	MOSFET Threshold Voltage	N/A		-
1025	Dose Rate Response of Linear Microcircuits	Mod*	Simulation Correlation	Address in Design/EI Tests, Relate to application.
1026	Preseal Burn-In	Ret		Address in Design/EI Tests, Relate to application.
1027	Thin Film corrosion Test	N/A		For marginal devices/conditions.
1028	Soft Error Test Procedure	Ret	Simulation Correlation	Design/Electrical Test and SQC/QRA*: new methods?

\* Consider Surrogate Devices

\*\* ICWG Subcommittee (see 3.2.6)

TABLE 2. ANALYSIS OF MIL-STD-883C: TM 2000 SERIES

Method No.	Environmental Tests	VHSIC QRA Disposition	Comments	Additional Comments of Task 2
2001	Constant Acceleration	Mod*	Consider Larger Packages	Assembly: consider for design evaluation.
2002	Mechanical Shock	Mod*	Consider Larger Packages	Assembly: design eval./relate to application.
2003	Solderability	Mod*	Consider Larger Packages	-
2004	Lead Integrity	Ret*	Consider Larger Packages	-
2005	Vibration Fatigue	Mod*	Consider Larger Packages	-
2006	Vibration Noise	N/A		-
2007	Variable Frequency Vibration	Ret		Assembly and SQC/QRA: relate to application.
2009	External Visual	Mod	Ambiguous Criteria	Assembly and SQC/QRA: Find more quantitative tests.
2010	Internal Visual (Monolithic)	Mod	Limited Application/ Ambiguous Criteria	Assembly and SQC/QRA: Find more quantitative tests.
2011	Bond Strength (Destructive Bond Pull Test)	Ret*		-
2012	Radiography	Ret		-
2015	Resistance to Solvents	Mod*	Review Stress Tests	Assembly
2016	Physical Dimensions	Ret		-
2018	SEM Inspection	New		Fab: mostly for metal; new techniques?
2019	Die Shear	Mod*	Review Stress Tests, Limited Application	-
2021	Glassivation Layer Integrity	Mod*	Review Stress Tests	-
2022	Micrograph Solderability	Mod*	Consider Larger Packages	Assembly: address VHSIC applicability
2023	Non-Destructive Bond Pull	Ret*		-
2025	Adhesion of Lead Finish	Ret*		-
2026	Random Vibration	Mod*	Consider Larger Packages	-
2027	Substrate Attach Strength	Mod*	Consider Larger Packages, Limited Application.	Assembly: consider for design evaluation.

\* Consider Surrogate Devices

### 2.3.2.3. Discussion of 3000 Series

#### o General

The 3000 series electrical test methods of MIL-STD-883C were reviewed next. Table 3 shows the VHSIC QRA disposition. It has been recommended that most of the test methods be retained (RET) and that some of the tests could be done possibly on a surrogate device (\*). Other dispositions and the reviewers thoughts are discussed below. Several new test methods were proposed and drafts prepared as a result of this review. These drafts are included in Appendix B.

#### o TM3005

For complex CMOS circuits, to do DC power supply current measurements, that is checking the leakage currents, adds little value. A better measure of the chip's power consumption is the measurement of dynamic current conditions. This gives the user a better idea of total power consumption to be used for board and power supply design.

#### o TM3011

The output short circuit test is used to monitor the ability of the TTL output drivers to sustain a momentary short during transients such as power up. This could be a destructive test and may make little sense when complex CMOS circuits are used. If this test is deemed useful, then modifications should be made to clarify exactly how the test is to be performed and a safe time limit set for this test for CMOS technology.

#### o TM3013

The noise margin test as stated in MIL-STD-883 makes little sense for highly complex chip designs. It should be stated here that noise margin considerations are important; however, the current method of testing the chips is hard, error prone, and may make no sense for VHSIC parts. When one specifies the voltage levels for the input and output pins, the noise margins are implied, especially

TABLE 3. ANALYSIS OF MIL-STD-883C: TM 3000 SERIES

Method No.	Electrical Tests	VHSIC QRA Disposition	Comments
3001	Drive Source Dynamic	Ret	Add Dynamic Supply Current Test
3002	Load Conditions	Ret	
3003	Delay Measurements	Ret	
3004	Transition Time Measurement	Ret*	
3005	Power Supply Current	Mod	
3006	High Level Output Voltage	Ret*	
3007	Low Level Output Voltage	Ret*	
3008	Breakdown Voltage, Input/Output	Ret*	
3009	Input Current, Low Level	Ret*	
3010	Input Current, High Level	Ret*	
3011	Output Short Circuit	Ret*	
3012	Terminal Capacitance	Mod*	
3013	Noise Margin Measurements for Digital Microelectronics Devices	Mod	
3014	Functional Testing	Mod	Update for Complex Functions Voltage Level/Machine Controversy
3015	ESD Sensitivity Classification	Mod*	
3016	Activation Time Verification	N/A	

\* Consider Surrogate Devices

if TTL compatibility is required. That takes care of the DC noise margin. If one is interested in the AC noise margin, which is really the sensitivity to narrow pulse widths, then a simple surrogate could be used or simulation could be used. Testing the AC noise margin even with a simple circuit at pulse widths of subnanoseconds does not lend itself to Automated Test Equipment (ATE) and is very error prone.

- o TM3015

In the ESD testing area for SSI and MSI devices, there has been constant controversy as to the accuracy of various tests and test equipment, whether the test is destructive, and what the voltage level classifications mean. We agree that electro-static sensitive circuits should be protected, but that seems to be the only agreement. In general, for VHSIC/VLSI, the devices are more susceptible to ESD damage than the larger geometry devices currently in inventory. While I/O protection circuits reduce ESD susceptibility, their use results in diminished performance (at VHSIC clock frequencies). Therefore, the ESD protection/performance tradeoff must be evaluated.

- o TM3016

This test method needs to be updated to address today's technology where activation items are shorter.

#### 2.3.2.4. Major Findings in 3000 Series

- o General

The test methods, in general, accurately describe those tests necessary to measure DC parameters and to perform AC type measurements. The automated test equipment (ATE) in today's technology is capable of performing most of the tests described automatically and without the need of modification. Since many of these tests are not time consuming on ATE, there may be little value in considering alternative approaches, such as surrogates. There are others, however, such as transition time measurements which can



be very time consuming. Alternative techniques should be considered for these tests.

General comments are summarized below:

- Test Methods, 3000 Series address for SSI issues and rely on manual testing
- Updates are needed to include test methods for the following:
  - . Set Up and Hold Times
  - . Tri-State Related Measurements
  - . Bidirectional Pin Measurements
  - . Min and Max Frequency Measurements
  - . Clamp Voltage Test
- o TM3005

The power supply current measurement method should include techniques to measure dynamic current especially of CMOS devices.
- o TM3011

The output short circuit test should be eliminated from those tests which are required in the VHSIC procurement specification.
- o TM3013

The noise margin situation is a very important issue, however, modern techniques when applied to this problem can reduce or eliminate this test. The use of careful procurement specification for the DC voltage pin parameters can, along with design CAD and DC pin testing, eliminate the DC noise margin test as currently stated in the military documents. The AC noise margin of today's circuits is the sensitivity of the device to subnanosecond pulses, which can be easily simulated rather than tested.

o TM3015

More discussion between the producer and user communities is needed to better define the type of test, test equipment, and classification.

o TM3016

The reviewers see limited need for this test method since the acquisition times are shorter for newer technologies.

o New Test Methods Needed

Electrical test methods which need inclusion to the MIL-STD-883 are summarized here (see Appendix B for draft versions of these test methods).

- Set Up and Hold Time

Set up and hold time tests for circuits that have flip-flops at the input edge of the chip need to be incorporated. This is a critical parameter when interfacing to other circuits and clocks on a printed circuit board. These parameters become very critical especially in high speed parts when their magnitude is only a few nanoseconds.

- Tri-State Related and Bidirectional Pin Measurements

Many complex chips are designed with tri-state pins either to interface bidirectional buses or because of the need to multiplex pins. Test methods to measure the transitions from high impedance to low impedance and in reverse becomes important in these high speed data systems. Also there may be requirements to hold the high impedance state level to a certain magnitude. This parameter should also be checked.

- Clamp Voltage

This test is used by many of the ATEs to check proper probe contact during wafer probe. This test should be done uniformly and standardized.

- Frequency Measurements, Minimum and Maximum

The maximum frequency of the chip should be known so that the user can be assured that the chip operation is not near the specification limit. The minimum frequency of the chip should be known when one is designing the chip using dynamic logic or any logic that needs periodic refreshing.

2.3.2.5. Discussion of 4000 Series

The review of the 4000 series test methods of MIL-STD-883 showed that most tests were intended for single or dual operational amplifier testing which is a serious hindrance when trying to apply these methods to highly complex chips and automated test equipment. Analysis results are shown in Table 4.

Today's technology allows many complex analog functions and even analog and digital functions on the same substrate. New and modified test methods must be found to adequately test these devices. Off-line surrogate testing of simple devices could be used to characterize some of the analog cells used in more complex designs.

2.3.2.6. Major Findings in 4000 Series

The reviewer's conclusion is that the methods stated in the current document are fine for what they were intended. However, new methods are needed to test complex analog and analog to digital converters.

Comments are summarized below:

- o Parameters measured are all valid
- o Test Methods 4000 Series address SSI and manual testing
- o Update for ATE and VHSIC level complexity needed
- o Update should include:
  - A/D and D/A devices
  - Incorporation of digital test methods

TABLE 4. ANALYSIS OF MIL-STD-883C: TM 4000 SERIES

Method No.	Electrical Tests	VHSIC QRA Disposition	Comments
4001	Input Offset Voltage and Current and Bias Current	Mod*	Consider ATE, and Analog and Digital on Same Chips
4002	Phase Margin and Slew Rate Measurements	Mod*	Consider ATE, and Analog and Digital on Same Chips
4003	Common Mode Input Voltage Range	Mod*	Consider ATE, and Analog and Digital on Same Chips
4004	Common Mode Rejection Ratio	Mod*	Consider ATE, and Analog and Digital on Same Chips
4005	Supply Voltage Rejection Ratio	Mod*	Consider ATE, and Analog and Digital on Same Chips
4006	Open Loop Performance	Mod*	Consider ATE, and Analog and Digital on Same Chips
4007	Output Performance	Mod*	Consider ATE, and Analog and Digital on Same Chips
	Power Gain and Noise Figure	Mod*	Consider ATE, and Analog and Digital on Same Chips
	Automatic Gain Control Range	Mod*	Consider ATE, and Analog and Digital on Same Chips

\* Consider Surrogate Devices

#### 2.3.2.7. Discussion of 5000 Series

The 5000 series of test methods serve several functions. For the most part, these are procedures (or Road Maps) rather than methods (Cook Books). More simply put, the 5000 series provides a listing of the tests and screens to be performed in chronological order.

Methods 5001 and 5002 are mathematical formulae for determining parameter mean value and distribution. These are well established and therefore should be useful for VHSIC/VLSI devices.

- o TM5003

Method 5003 provides the flow for microcircuit failure analysis. The procedure described is sound and reasonable for VHSIC/VLSI. Some valuable techniques have been developed since the last revision and should be considered for inclusion (eg., IR Scan, AUGER). It should be noted that many of the faults that have been easily detectable through optical examination will be detectable at best using SEM for VHSIC/VLSI. The problem is then one of isolating the functional/electrical fault to a minimum of chip real estate. It is therefore recommended that fault isolation circuitry, perhaps built-in test (BIT), be considered.

- o TM5004

Method 5004 Screening Procedures are well established and proven. It is desirable to retain these screens. In cases where Parametric Monitor (PM) or Standard Evaluation Circuit (SEC) data allows parameters to be guaranteed by design, their use will be recommended in place of actual devices or as a complement to actual device screening. The QML approach is intended to eliminate devices of low quality and reliability in the early phases of design, fabrication, and assembly. This will greatly reduce the fallout during screening.

- o TM5005

Method 5005 Quality Conformance and Qualification Procedures serves as the road map for current qualification of microelectronic circuits. A similar document will be necessary to establish

qualification procedures for VHSIC/VLSI under the QML. Use of surrogate devices for all destructive testing should be given consideration. This approach is already in place (e.g., use of electrical rejects for bond pull, die shear) but needs to be expanded since VHSIC/VLSI material lots are of significantly low volume and do not lend themselves to samples sizes currently required. In addition, the use of high cost VHSIC/VLSI devices for destructive tests is not cost effective. Therefore, the use of surrogate devices and the development of better prevention techniques and in-line screening is recommended over end-of-line testing.

o TM5006

Method 5006 has the purpose of determining the maximum capabilities and limitations of a device. Modifications should be made to relate these important device characteristics to process and design parameters which can, in turn, be derated. This will ensure that adequate margins of operation are defined to enhance overall reliability.

o TM5007

Along with an emphasis on detecting failure early in fabrication/assembly, a set of requirements should be considered to assess the quality of a wafer lot. Method 5007 currently uses sample testing of potential finished products to determine lot acceptance. The testing is primarily physical (i.e., optical, SEM examination). Method 5007 should be modified to measure primarily parametric monitors (PMs) by means of electrical or other quantitative tests. This requires a comprehensive set of PMs.

o TM5010

Method 5010 has many good elements suitable for a VHSIC/VLSI Quality and Reliability Assurance program since it addresses low volumes which are related to custom devices and VHSIC/VLSI. The low volume/high price issue is the driving force to utilize

surrogate devices in QCI since a much broader quality database can be drawn from QCI of the same design, lot after lot.

2.3.2.8. Major Finding in 5000 Series

- o Method 5010 has many good features applicable to VHSIC/VLSI screening and QCI.
- o Use of surrogate devices is desirable for destructive testing. A summary of the comments for the 5000 Series of test procedures is given below:
- o Destructive testing (5006, 5009) mandates use of SECs.
- o Failure analysis (5003) could be enhanced by incorporation of BIT, and modern analytic tools.
- o For VHSIC devices, screening and qualification procedures could be incorporated in TM 5010.

2.3.3. MIL-STD-976A

2.3.3.1. Discussion of MIL-STD-976A

MIL-STD-976A, Certification Requirements for Microcircuits, establishes the requirements which must be met by a manufacturer during an audit. It addresses technology up to the LSI level and does not address design issues. The technology of today is characterized by high density, high cost, submicron feature sizes and low process yields.

The following areas need to be addressed in Mil-Std-976:

- o Use of surrogate devices.
- o Address design function.
- o Clarify what constitutes a Major or Minor process change.

- o Need to provide direction to Industry on Foundry concept and how to deal with multi-group QML certification.
- o A "Road Map" or some other method is required to better utilize the interaction between referenced documents.
- o Include state-of-the-art process control techniques in areas of Mask Fabrication and highly sensitive process steps.

#### 2.3.3.2. Major Findings in MIL-STD-976A

Stress testing of actual circuits should be reviewed for cost effectiveness and value. Use of surrogate devices and emphasis on process control rather than individual product stress testing should be considered.

Areas that require revamping will be reviewed by the ICWG to provide a document that not only leads to certification but also allows industry to improve their processing capabilities in the areas related to yields and quality. Clarification of a major or minor changes is critical.

#### 2.3.4. MIL-STD-1331

##### 2.3.4.1. Discussion of MIL-STD-1331

This document describes the parameters required as a minimum for the specification of microcircuits during the 1960s. The purpose was to provide minimum parameters (independent of the circuit design), abbreviations, definitions, and symbols, which are necessary for the evaluation of the circuit design and procurement of the microcircuits.

It refers to the following documents:

Specification Military:

MIL-M-55565 Packaging of Microcircuits



#### Standards Military:

MIL-STD-806 Graphic Symbols for Logic Diagrams

MIL-STD-883 Test Methods and Procedures for Microelectronics.

MIL-STD-1313 Microelectronic Terms and Definitions.

Although the purpose of this document was to make it independent of the circuit design, the definitions and related terminology did not keep up with the evolution of technology. For example, today's packages with their vast number of pin-outs require different approaches. Also, this document does not define terms, such as gate delays, propagation delay as a function of temperature, or supply voltage as well as the parameters related to modern VHSIC/VLSI and Analog-to-Digital/Digital-to-Analog Converters.

#### 2.3.4.2. Major Findings in MIL-STD-1331

This document is useful and needs to be updated, seeking help from sources like IEEE Standards Dictionary, ANSI and NBS Standards. It was a unanimous decision that this document needs a thorough overhaul.

#### 2.4. SUMMARY

The Task 1 team performed a thorough review and analysis of the current military standards and specifications that pertain to the manufacture of microcircuits. Each document was evaluated for its applicability to the generic qualification approach of complex microcircuits and recommendations were made as to whether a document was appropriate as is or needed to be modified, or replaced. In the area of electrical tests the need for several new methods was identified.

### 3. TASK II - INVESTIGATION

#### 3.1. INTRODUCTION

The investigation task had two major objectives. The first objective was to obtain the cooperation and participation of the microcircuit industry in identifying the methods to be used for generic qualification of microcircuits. The second objective was to draft a set of specifications defining requirements for obtaining a Qualified Manufacturer's List (QML) listing.

The first objective was met through the establishment of an Industry Coordinating Working Group (ICWG) composed of representatives of the manufacturers and users of microcircuits.

The second objective was met by the contract team of GE, AT&T, and Honeywell through a series of working sessions in cooperation with the RADC program office. This effort produced a detailed draft of QML requirements which was then submitted to the ICWG for review and comment.

#### 3.2. INDUSTRY COORDINATING WORKING GROUP (ICWG)

A key aspect of the program was the establishment of a technical group to discuss issues related to controlling quality and reliability through process control. This group was the Industry Coordinating Working Group (ICWG) and consisted of 90 individuals from government, manufacturing, users and academia. The charter of this group was to insure maximum industry technical input, applicability, concurrence and utility of the proposed QRA procedures.

##### 3.2.1. ICWG Organization

The ICWG was divided in five subcommittees to help facilitate the discussions. These subcommittees were: Quality Management, Design, Fabrication, Assembly/Packaging, and SQC/QRA.

The first meeting of the ICWG was held in February 1987. At this meeting the entire ICWG met and listened to presentations on the task of developing new qualification procedures for microcircuits. This new procedure had been given a name by that time and was known as Generic Qualification. The application of Generic Qualification became known as the Qualified Manufactures Listing (QML). After the general session the ICWG divided into the five subcommittees and initiated their discussions.

The various subcommittees met throughout 1987 and provided technical solutions to the problems associated in implementing a quality/process oriented qualification system. These inputs included: Standard Evaluation Circuit (SEC), Technology Characterization Vehicle (TCV), Technology Review Board (TRB), SPC, Total Quality Management (TQM) and other significant concepts which were readily adaptable to the QML. Further discussion on the output of the subcommittees follows.

### 3.2.2. Quality Management ICWG Subcommittee

The main objective of this subcommittee was to discuss quality management implementation issues, and feasibility and cost effectiveness of the proposed technical outputs of the other subcommittees. Most members of this subcommittees actively participated in the other subcommittees, thus this group became more of an overseer and coordinator of the other four subcommittees.

### 3.2.3. Design and Test ICWG Subcommittee

#### 3.2.3.1. Topics of Discussion

The design subcommittee was organized to address design techniques and CAD tool control related to certification and qualification. The design process, especially those using CAD tools had never been included in the quality audit function. The major obstacle was to develop procedures which document the design process without limiting flexibility. There was a great deal of concern that design creativity might suffer as a result of the implementation of quality controls.

The discussions in the Design and Test ICWG subcommittee meetings included the following topics:

- o Design Rules
- o Electrical Rules
- o Cell Libraries
- o Testability
- o Layout
- o Test Generation
- o Design Transfer Procedures
- o Test procedures
- o VHDL/TISSS
- o Electrical tests

#### 3.2.3.2. Major Results

The Design and Test ICWG Subcommittee focused on quality and reliability issues concerning the microcircuit designer and the wafer test facility personnel. This subcommittee met four times with each meeting attended by 20 people representing industry, DoD, and other government agencies. The following items received the most attention at the meetings:

- o Fault Coverage - There was never any general agreement that a high percentage of fault coverage (over 95%) was achievable. However, it was agreed that it was necessary. A requirement has been established by DoD through MIL-STD-454 Requirement 64 to have at least 98% fault coverage on all VHSIC and ASIC devices, designed after Sep 88. Discussions concentrated on how to achieve and monitor this level of fault coverage.
- o Device specification - There were two major issues. One issue involved the transfer of responsibility for writing the document from DESC to the supplier. In the QPL method slash sheets were always prepared by DESC. In the QML method, it was proposed that the vendor prepare the specification and have DESC approve it. The second issue involved the format and nature of the information in the device procurement specification. This discussion had extremes from very simple functional specification to a very

detailed specification containing test requirements, package requirements and screening requirements. As the program progressed, the following requirements for the device procurement specification, which now reside in MIL-I-38535, were established: Absolute maximum ratings; recommended operating conditions; electrical performance characteristics; electrical test requirements; functional description; burn-in circuit; quality assurance provisions; packaging requirements; and device package marking requirements.

- o CAD/CAE Software Verification - One approach was to write a standard set of benchmarks and certify all design tools against those benchmarks. It was quickly determined, that standard benchmarks would not work even with the same tools located in two different locations. A more reasonable approach was to ascertain, through documented evidence, how each supplier maintained control of their software tools and verified new software before releasing it to production. In addition, a manufacturer should have documented evidence of benchmark testing for "checking software"; such as a Design Rule Checker (DRC), Electrical Rule Checker (ERC) and Layout Versus Schematic (LVS). A comprehensive document describing what must be done to validate a software system was developed. This document, entitled "Requirements to Qualify CAD Tools for VHSIC Devices" is included as Appendix C of this report. Many of the ideas from this document were adopted in MIL-I-38535.
- o Accuracy of Models - The initial goal was to set some accuracy standards for model performance parameters. This idea was firmly rejected in favor of comparing the simulated parameter results of actual devices and the SEC to the actual performance parameters. If the performance of these devices stay within the device specification limits, then the models are assumed to be predictable within acceptable limits.

- o Test Methods from MIL-STD-883 - In general, the actual execution of all AC timing measurements and many DC electrical tests of VLSI chips require the extensive use of functional test vectors for initialization and setup. In the realm of VLSI systems-on-a-chip, the concepts and definitions of propagation delay, setup times and hold times involve a level of complexity which is not adequately addressed by the existing procedures. The following test methods were discussed and recommendations were made;

Modify:

Method 3005 Dynamic Power Dissipation (Addendum).

Method 3006 High Level Output Voltage Measurement.

Method 3007 Low Level Output Voltage Measurements.

New Procedures: (see Appendix B for draft versions of these test methods)

Method 30TS-1 Set-Up Time Measurements.

Method 30TS-2 Hold Time Measurements.

Method 30XX Minimum Pulse Width Measurement.

Method 30YY Wafer Probe Contact Test.

Method TPZ.1 Tri-State Propagation Delay Measurements

Develop Analog Test Methods:

The complete 4000 series analog test methods need to be updated to consider modern automated test equipment.

### 3.2.4. Fabrication ICWG Subcommittee

#### 3.2.4.1. Topics of Discussion

The wafer fabrication community was already familiar with the requirements for certification per MIL-STD-976A; thus the primary focus of the ICWG was to introduce the new concepts required for generic qualification.

Typical discussion topics for the Fabrication ICWG subcommittee meetings were as follows:

- o Parametric Monitor (PM)
- o Standard Evaluation Circuit (SEC)
- o Technology Characterization Vehicle (TCV)
- o Technology Review Board (TRB)
- o Statistical Process Control (SPC)
- o Quality Assurance Plan

#### 3.2.4.2. Major Results

The Fabrication ICWG subcommittee addressed the methods needed to control a wafer fabrication line guaranteeing high quality, high reliability material without the necessity of full qualification and reliability tests on samples of each device type manufactured. The concept of encouraging continuous improvement instead of demanding strict adherence to a certified process was also introduced.

The following items contain the major results of the Fabrication ICWG subcommittee meetings:

- o Parametric Monitor - The concept of the Parametric Monitor evolved from the need to have structures on each wafer that can be used to determine if the circuits on that wafer can be expected to yield satisfactory devices. Initially this collection of structures was referred to as a Process Control Monitor. The word control was dropped since these structure are intended for end of line testing and therefore do not contribute to "control" of the process. The word "process" was changed to "parametric" in order to reflect the actual use of the structures. The conclusion was that each wafer must contain PMs either as kerf structures or drop-in sites that can be electrically tested for use in wafer acceptance. These test sites can be used for monitoring the simulation model parameters used to predict the electrical performance of the circuits being fabricated.

The subcommittee also discussed whether specific structures should be required in each manufacturer's PM. It was concluded that each manufacturer should design their own PMs which address and monitor specific electrical parameters which were deemed critical. These structures along with their test plan and justification are submitted to the qualifying activity for approval.

- o Standard Evaluation Circuit - The requirement for the periodic processing and life testing of a Standard Evaluation Circuit was the most controversial subject addressed by the subcommittee. The discussions revolved around four fundamental issues: the required complexity and functionality of the SEC, the use of a standardized SEC, the design methodology of the SEC, and the frequency of manufacture.

The SEC complexity and functionality issue centered on the desire for the SEC to be a saleable device so that the manufacturer could recover some of the costs associated with its fabrication. It was concluded, however, that some sort of bit mapping capability in the SEC is needed to aid in failure analysis and fault detection. These factors pointed to the use of a memory chip for the SEC even though memory chips usually employ unique design techniques that would not be representative of all ASIC's.

The final recommendation was that the manufacturer needed to establish the SEC complexity and functionality within the guidelines that the SEC was at least one half the complexity of the most complex device he expected to design within the technology. An actual product could be used as a SEC provided it met the SEC guideline requirements.

The use of a standardized SEC was found to be impractical since processes and materials used by various manufacturers vary widely.



Even if a standardized SEC was used it would be difficult for one to compare results. It was decided that the manufacturer was the best one to define, specify and evaluate the SEC for overall effectiveness to assess the technology.

The design methodology discussion determined that the SEC design methodology must exercise the technology minimum design rules in a significant proportion of the device.

The frequency of SEC fabrication and testing issue was complicated by the diversity of fabrication volumes among the various manufacturers. It was finally recommended that each manufacturer be allowed to establish the frequency of SEC fabrication that, in his judgement, would provide sufficient proof that his process was being maintained within proper limits. However, in no circumstance should the period between SEC fabrication lots exceed 12 months. Paramount in a manufacturer's business decision in selecting the frequency of SEC fabrication would be the amount of product he would place "at risk" should the SEC fail to pass reliability test.

- o Technology Characterization Vehicle - The Technology Characterization Vehicle brings together the structures necessary to determine a technology's intrinsic reliability characteristics. These structures will normally be used to bring up a new process and provide data on electromigration, time dependent dielectric breakdown, and hot carrier effects. In the QML environment it will be necessary to process and test the TCV structures periodically to insure that the intrinsic reliability of the product is being maintained.
- o Technology Review Board - The Technology Review Board was first introduced as a mechanism to control the wafer fabrication line. It has evolved into the primary control organization for the entire manufacturing line. The TRB is responsible for the quality

of the product and has the authority to make changes in the process when sufficient data has been obtained to justify the change. This authority is the way that continuous improvement in quality can be obtained within the framework of a qualified process. The establishment of the TRB was seen by the subcommittee as a formalization of the way most companies tended to operate in order to address the total effect of any changes on their manufacturing process.

### 3.2.5. Assembly/Packaging ICWG Subcommittee

#### 3.2.5.1. Topics of Discussion

The Assembly/Packaging subcommittee was responsible for recommending and evaluating aspects of the back-end processing steps. The Hybrid community had just successfully started process qualification using MIL-STD-1772 and close scrutiny was maintained as similar issues existed in various process steps.

Typical discussion topics at the various Assembly/Packaging subcommittee meetings included:

- o Standard Evaluation Circuit (SEC) Package
- o Design/Fabrication/Assembly Interface
- o Package Technology Style Qualification
- o Off-Shore Suppliers
- o Statistical Process Control (SPC)
- o Quality Management (QM)
- o Technology Review Board (TRB)
- o TAB/Flip-Chip Technology
- o Screens and Test Methods
- o Multi-Chip Packaging

#### 3.2.5.2. Major Results

The Assembly/Packaging ICWG subcommittee quickly realized that some of the concepts associated with Generic Qualification were not implemented in the Assembly process the same way as in Design and Wafer Fabrication.

The following items highlight the activity of the Assembly/Packaging subcommittee:

- o Package Technology Style Qualification - The need to have a Generic Qualification approach for the assembly line was readily agreed upon. At the same time there was a need to replace the surrogate package concept with a more practical approach. All agreed that too many package types exist to maintain a constant flow of each family using the SEC.

The concept of Package Technology Style Qualification was introduced and developed. All agreed that custom package design would always exist and extensive package qualification would probably be required; but, in those instances where a technology style of packages could be developed, a great benefit would be realized if some of the package qualification procedures could be combined for similar packages. The Package Technology Style concept requires thorough testing and characterization of a particular package technology style. As variations of the tested package were used, only those tests required to ensure that quality and reliability were maintained need be retested. Once a technology style of packages is defined and as more variations of that package style are used, fewer additional tests would be required because of similarities in package characteristics.

An extensive table of technology style variation versus required retest was developed for discussion but was later removed and left to the manufacturer to have his plan validated by the qualifying activity. A copy of the table is in the August 1988 draft of the proposed Generic Qualification document .

- o Statistical Process Control (SPC) - With the concept of built-in quality and reliability, the assembly process would need to include SPC. Since many assembly/packaging steps were being automated, these automated procedures would require full

characterization and SPC control by skilled trained operators. SPC provides the tools to monitor the ongoing performance. If proper limits are used, then yields would be improved. Areas identified for SPC included, but was not limited to; incoming assembly process materials; incoming package acceptance; equipment used for assembly; wafer acceptance criteria; die attach; chip to package interconnect; package seal; marking; rework; lead trim, form and final finish; atmosphere and cleanliness control.

- o Screens and Test Methods - The majority of the discussions in the Assembly/Packaging ICWG meetings centered around back-end testing. This included screens and qualification testing. The goal was to reduce testing time and costs, while enhancing the quality and reliability of products. The committee began by drafting specific requirements that would meet all types of assembly processing.

Due to the broad spectrum of individual contributors, it soon became apparent that guidelines must be proposed and individual manufacturers would need to establish, verify and qualify each individual plan. The ownership of the screens and test methods would be jointly shared by the individual manufacturer and qualifying activity. MIL-STD-883 was accepted as the vehicle to control the screens and test methods, but the manufacturer was responsible to verify that the MIL-STD-883 testing enhanced his product's quality and reliability. This also meant that in-line control could replace in part or in total some testing requirements.

Due to the increased performance expectations and shrinking physical size of interconnect lines on packages, new test methods were required. The Assembly/Packaging committee endorsed the use of three new Test Methods; 3017, 3018 and 3019, for chip/package testing.

TM 3017, "Microcircuit Package Digital Signal Transmission", provides testing for transmission line characteristics of packages when performance and complexity warrant such testing as determined by the manufacturer.

TM 3018, "Crosstalk Measurements for Digital Microelectronic Device Package", addresses the crosstalk of high performance signals in the package environment.

TM 3019, "Ground and Power Supply Impedance Measurements for Microelectronic Device Package", provide proper testing of package power and ground designs for high performance applications, when deemed necessary by the manufacturer.

- o Technology Review Board (TRB) - The role of the Technology Review Board (TRB) was determined to be to review and approve the assembly quality assurance plan and monitor its on going success. SPC data could be presented to justify a particular manufacturer's approach to process control. As an example, SPC data showing the control of moisture content in the seal environment may result in changes to the requirement for moisture content testing later in the testing cycle.

### 3.2.6. SQC/QRA ICWG Subcommittee

#### 3.2.6.1. Topics of Discussion

The role of the SQC/QRA ICWG subcommittee was to address reliability and quality issues as they pertained to QML. Although a stand alone subcommittee, SQC/QRA issues were integrated through all ICWG subcommittees, with up front implementation of quality and reliability to "build-in" quality and reliability.

Typical SQC/QRA ICWG subcommittee discussion topics included:

- o Design issues including electrical test methods, cell library certification, configuration control and CAD tool certification.
- o Fabrication issues including proposed PM parameter list, SEC requirements, wafer lot acceptance, initial qualification, ongoing monitoring and change control.
- o Packaging/Assembly issues including package qualification, assembly validation and operator training.
- o SPC for fabrication and packaging/assembly.
- o Device quality, quality conformance and screening.
- o Quality Management (Quarterly Report and TRB)

#### 3.2.6.2. Major Results

The SQC/QRA subcommittee supported the use of the SEC and PM program in the Fabrication subcommittee to allow for initial line qualification and ongoing qualification testing to ensure technology quality and reliability. In addition, Statistical Process Control (SPC) was included to further identify process control in the fabrication and assembly processes. Yield related failure mechanisms were identified including electromigration and hot carrier aging. After an attempt to identify standard structures to be used, the SQC/QRA subcommittee agreed to have the manufacturer identify and validate his structures to address these failure mechanisms. QML requires two (2) steps to be completed. First, validation of the manufacturer's quality management plan by the qualifying activity. Second, qualification is obtained by successfully demonstrating through design, fabrication, assembly and testing of the SEC along with two (2) additional designs. Ongoing maintenance and reporting of QML status was established through two forms of Quality Conformance Inspection (QCI) and a reporting process through use of a Quarterly Report written by the TRB.

### 3.3. DRAFT OF QML REQUIREMENTS - APRIL '88 DRAFT

As a result of the document reviews and inputs from the ICWG, the contract team drafted a single document that outlined the requirements for setting up and maintaining a microcircuit manufacturing line based on certifying and qualifying the processes. Successful completion of these requirements would result in placement on the Qualified Manufacturer's List (QML). The document encompassed the entire manufacturing technology flow within the following format.

#### Introduction

Section A	-	General Requirements
Appendix 1 of A	-	Quality Assurance Program
Appendix 2 of A	-	Statistical Sampling, Test and Inspection Procedures
Appendix 3 of A	-	Device Specification Requirements
Appendix 4 of A	-	Statistical Process Control Plan
Section B	-	Requirements for Line Certification (Generic Qualification)
Appendix 1 of B	-	Quality/Reliability Vehicle Requirements
Appendix 2 of B	-	Audit Checklist for QML Microcircuit Certification
Section C	-	Qualification Requirements for Complex Monolithic Microcircuits
Method XXXX	-	Test Procedures for QML'd Monolithic Microcircuits
Appendix 1 of X	-	Wafer Acceptance
Appendix 2 of X	-	Package Qualification Procedures

In April of 1988 the first draft of the Generic Qualification document was released for review and comment. This document followed the outline given above and was coordinated by RADC/RBRA. The intent was to present QML implementation requirements for microcircuits to the industry for comment and critique. The intent of Generic Qualification for QML is to give the manufacturer needed flexibility and responsibility to control and improve the high quality and reliability of his product.

The following technical considerations were incorporated into the first draft document to address the reliability issues of an QML manufacturing environment:

- o Manufacturer's QA Program Plan
- o Self Audits
- o Technology Review Board (TRB)
- o Total Quality Management/Control (TQM/TQC)
- o Statistical Process Control (SPC)
- o Standard Evaluation Circuit (SEC)
- o Quarterly Reports

These key concepts are briefly discussed in the following paragraphs.

### 3.3.1. Manufacturer's QA Program Plan

The QA Program Plan for QML continues to be the vehicle whereby the manufacturer maintains control over the quality of his product.

#### 3.3.1.1. QA Program Plan-Section A

As a precondition to qualification, the microcircuit manufacturer shall establish and implement a quality assurance program. The Quality Assurance Program Plan shall be submitted to the Qualifying Activity as part of the certification process.

After a manufacturer receives qualification, he shall not implement any change in microcircuit design, material, process or control without concurrent change in the quality assurance program documentation. Changes



made to the process control or quality control documents listed in the approved Quality Assurance Program Plan shall be reported to the Qualifying Activity.

The manufacturer shall be actively developing an SPC program and an expected date of a full program institution shall be indicated as part of the Quality Assurance Program plan.

The qualifying activity has the right to remove the QML status of a line for failure to meet or maintain compliance to any requirements or failure to meet the Quality Assurance Program Plan submitted as part of Certification.

The QA Program Plan shall identify minimum loading required to maintain quality and reliability of the manufacturer's line.

Life Tests shall be performed on the SEC at intervals set by the TRB in the Quality Assurance Program Plan.

Microcircuits shall be manufactured, processed, and tested in a careful and workmanlike manner in accordance with good engineering practice, within the requirements of the QML specification, and within the production practices, workmanship instructions, inspection and test procedures, and training aids prepared by the manufacturer in fulfillment of the quality assurance program.

#### 3.3.1.2. QA Program Plan-Appendix 1 of Section A

As a guide to implementing a QA Program Plan, Appendix 1 of Section A was included.

The manufacturer's quality assurance program shall demonstrate and assure that design, mask making, fabrication, assembly, inspection and testing of microcircuits is adequate to assure compliance with the applicable requirements and quality standards of the QML document. When any portion of

the design, fabrication, assembly and testing operation is other than at the manufacturer's facility, it shall be the responsibility of the manufacturer to secure and prove the documentation and control of the quality assurance program of the other location.

All required quality assurance program documentation and records shall be available for review by the qualifying activity upon request.

The QA Program Plan shall be established and maintained by the manufacturer, and shall be delivered to the qualifying activity for review prior to the certification audit. It shall consist of a volume or portfolio, which will serve to demonstrate to the qualifying activity that the manufacturer's understanding of a complete quality assurance program, as exemplified by his documentation system, is adequate to assure compliance with the applicable specifications and quality standards. If the quality assurance program exemplified is applied consistently to all product lines intended to be submitted for acceptance inspection under the QML document, only one program plan is required for each manufacturing plant; any difference in treatment of different product lines within a plant shall be stated and explained in the program plan, or separate program plans prepared for such different lines. The program plan shall contain, as a minimum, these items:

- o Functional block organizational chart.
- o Example of design and manufacturing flow chart.
- o Proprietary-document identification.
- o Examples of design, material, equipment, visual standard, and process instructions.
- o Examples of records.
- o Examples of design, material and process change control documents.
- o Examples of failure and defect analysis and feedback documents.
- o Examples of corrective action and evaluation documents.
- o Manufacturer's internal instructions for internal visual inspection.

- o Examples of test travelers.
- o Examples of design and construction baseline.
- o Manufacturer's self audit program (see paragraph 30 herein).

#### 3.3.1.3. QA Program Plan-Section B

The manufacturer shall provide documentation showing evidence that their Quality Assurance Program Plan has been implemented.

#### 3.3.2. Self Audit

The manufacturer's self audit is an ongoing discipline that serves to maintain manufacturing quality by reviewing, improving and checking the manufacturers procedures for compliance to the QA Plan.

##### 3.3.2.1. Self Audit-Section A

The manufacturer's self audit not only helps maintain manufacturing quality but the self audit results are submitted to the qualifying activity at the time of certification as one of the means of certifying that all facilities, equipment, procedures, analytical tools, and documentation are appropriate for the manufacture of high quality, reliable, monolithic microcircuits.

##### 3.3.2.2. Self Audit-Appendix 1 of Section A

The intent of a self-audit program is to assure continued conformance to this QML specification and provide the qualifying activity a means of having precertification audit data.

The manufacturer shall establish an independent self-audit program under the direction of the TRB to assess the effectiveness of the manufacturer's compliance to all applicable specifications. The manufacturer's self-audit program which identifies key review areas, their frequency of audit, and the corrective action system to be employed when variations from the approved procedures or specification requirements are identified shall be included in the program plan. The self-audit program shall as a minimum incorporate the following requirements:

- o A system to identify and correct any deficiencies (e.g. design, processing and testing) or deviations from the QA Program Plan.
- o Provide for review of all deviations from critical documents such as baseline(s), flow chart(s), means of traceability, QCI procedures when applicable.
- o Specify the selection and training/retraining requirements for auditors.
- o Specify the self-audit frequencies and require that a schedule be established and adhered to.

The designated auditors shall be independent from the area being audited. If the use of an independent auditor is not practical, then as a minimum another individual should be assigned to participate in the audit or review the results with the auditor from the area. The auditors shall be familiar with the area to be audited, with the applicable QA Plan, and provided with an appropriate checklist for annotating deficiencies. Prior to the audit, the assigned auditor(s) shall review the previous audit checklist to assure corrective actions have been implemented and are sufficient to correct the deficiencies.

The self-audit checklist shall be approved by the TRB and maintained under document control. The checklist shall assure that the quality assurance system is adequate and followed by all personnel in each area.

### 3.3.3. Technology Review Board (TRB)

The TRB is the board appointed by the manufacturer, made up of representatives of each function in the manufacturing line, responsible for acquiring, maintaining, and reporting the status of the line to the Qualifying Activity.

#### 3.3.3.1. Technology Review Board-Section A

The organizational structure of the TRB shall be up to the manufacturer but the manufacturer shall submit the names, addresses, and phone numbers of the members of the TRB to the Qualifying Activity including a list of contact people. Any changes to the TRB shall be included in the quarterly report. Any change in the contact person or persons shall be reported to the Qualifying Activity immediately. Records shall be maintained of the TRB's membership, deliberations and decisions. Records shall also be kept of dissenting opinions of board members.

The TRB shall submit quarterly to the Qualifying Activity a Quarterly Status Report.

The manufacturer's Technology Review Board will judge the current status of the QA Program Plan and reliability of its microcircuits by review of the SPC and TQC status of the manufacturer's line, reliability test data (i.e., PM, TCV, SEC and device), the rate of board assembly failures and field returns, and the Failure Analysis (FA) results of screen and burn-in failures.

The frequency and testing methods for interim evaluations of the SEC and/or the TCV are to be determined by the TRB based on the manufacturer's assessment of risk. The manufacturer's interim SEC and TCV evaluation plan shall be documented.

When reliability of shipped microcircuits is called into question, the TRB shall provide quick evaluation and/or corrective action and prompt notification to the Qualifying Activity to preserve the manufacturer's qualified status.

All changes to any part of a QML'd manufacturers line are to be monitored (not necessarily formally approved) by the manufacturer's TRB, accompanied by changes in the Quality Assurance Program Plan when applicable, and available to the Qualifying Activity. In addition when applicable,

changes shall be documented as to the reason for the change with supporting data taken to support the change, including reliability data.

The decision as to the criticality of the change shall be guided by the potential effect of the change on quality, reliability, performance and interchangeability of the resulting microcircuits. For any change that merits consideration for requalification the TRB shall decide if requalification is needed. Microcircuits shall be shipped following a change only upon approval of the TRB following the review of data available to show that the change produces the required quality and reliable microcircuits.

The TRB shall maintain a Technology Characterization Vehicle (TCV) to be complete and accurate for all known intrinsic reliability failure mechanisms and report such status in the Quarterly Status Report.

Sampling for nonelectrical screens can be an acceptable substitute for any specified screening procedure provided that the sampling procedure and supporting data be documented and approved by the TRB and submitted to the Qualifying Activity.

A TRB representative shall verify screening, qualification and QCI records when corrective addenda affect lot jeopardy.

All self-audit reports will be filed and maintained by the TRB. The TRB shall establish a procedure to follow up on all audit deficiencies to assure that the corrective actions have been implemented in a timely manner.

The self-audit frequency shall be established with a schedule by the TRB but in no case exceed one year for each area, unless authorized by the Qualifying Activity.

The manufacturer shall demonstrate the process capability for the following areas of design:

- o Design simulation versus routing simulation

- o CAD routing and post-routing simulation
- o Design check software verification
- o Testability/fault coverage

Test plans for each of these areas shall be approved by the TRB and submitted as part of the Certification Test Plan. All tests shall be completed and documented before certification is granted.

The TRB shall determine the tests to be accomplished on the TCV, SEC, and PM and submit to the Qualifying Activity a test plan with parametric limits and accept/reject criteria. All elements in the database shall be in compliance with the geometric and electrical design rules approved by the TRB. Documented design rules consisting of geometric layout and electrical rules for wafer fabrication, approved by the TRB and implemented in the design of all QML microcircuits shall be documented and verified. The manufacturer shall control the environment of the QML wafer fabrication facility in terms of relative humidity, temperature, and particle count as specified by the TRB. The Qualifying Activity shall be shown evidence that each processed wafer in a wafer fabrication facility contains parametric monitors that include the parameter requirements specified and meet the pass/fail criteria for each parametric structure established by the TRB. Wire bond materials and equipment calibration, automatic and/or manual, shall meet the reliability criteria established by the TRB and approved by the Qualifying Activity. Tape-automated-bonding (TAB) materials and equipment shall meet the reliability criteria established by the TRB. The Qualifying Activity shall clearly identify the deficiency in the Audit Exit Report and obtain TRB signature verifying notification.

After the initial QML qualification process, the SEC shall be manufactured at least every 12 months, or more often as determined by the TRB. After initial certification/qualification, the TCV shall be manufactured and tested at least every 12 months, or more often as determined by the TRB.

#### 3.3.4. Total Quality Management/Control (TQM/TQC)

QML manufacturers shall maintain a system of Total Quality Control (TQC) intended to continuously improve the quality and reliability of the microcircuits produced .

##### 3.3.4.1. Total Quality Management/Control (TQM/TQC)-Appendix 1 of Section A

A company-wide total quality control (TQC) policy shall be adopted to describe top management's commitment to quality assurance. Quality assurance objectives shall be established for quality elements such as field performance and reliability levels, internal inspection quality standards, supplier quality assessment and personnel training/qualification.

Documentation is required on the wafer fabrication process including the SPC and TQC programs.

#### 3.3.5. Statistical Process Control-Section A

The manufacturer shall be actively developing an SPC program and shall describe and indicate in the Quality Assurance Program Plan the goals of the program. Failure to meet these goals can be grounds for removal from QML. The status of the SPC programs shall be reported quarterly in the status reports issued by the TRB.

##### 3.3.5.1. Statistical Process Control-Appendix 1 of Section A

The SPC program shall be documented and the means for collecting, recording and interpreting the data shall be described. Also, SPC training programs shall be discussed.

##### 3.3.5.2. Statistical Process Control-Section B

The manufacturer shall provide documentation and records, upon request, to the qualifying activity that critical nodes are under SPC or other in-process monitoring programs. Implementation dates for areas not under SPC shall be provided. For example, the PM measurements shall be used as part of the manufacturer's SPC program.



### 3.3.6. Standard Evaluation Circuit (SEC)-Section A

The manufacturer's Technology Review Board will judge the current status of the quality and reliability of its microcircuits by review of the SPC and TQC status of the manufacturer's line, reliability test data (i.e., PM, TCV, SEC and device), the rate of board assembly failures and field returns, and the Failure Analysis (FA) results of burn-in failures and board assembly and field returns. The SEC is a key test vehicle in assessing the reliability characteristics of the technology.

#### 3.3.6.1. Standard Evaluation Circuit (SEC)-Section A

The wafer fabrication process shall be monitored and controlled using a Standard Evaluation Circuit (SEC), Technology Characterization Vehicle (TCV) and Parametric Monitors (PM). The frequency and testing methods for interim evaluations of the SEC and/or the TCV are to be determined by the TRB based on the manufacturer's assessment of risk. The SEC and TCV data is to be used as a tool for monitoring the quality and reliability of the manufacturer's line and does not automatically disqualify a manufacturer when trends or limits require corrective action.

A summary of reliability test data, including SEC data, collected over the past quarter shall be included in the Quarterly Status Report. The results shall be compared with the current approved baseline data. If, at any time, there is a shortage of QML microcircuit designs available for manufacture on the QML'd line, the SEC and PM shall be continuously produced and tested along with Non-QML microcircuit designs.

A QML manufacturer shall process, screen and life test an SEC at intervals set by the TRB in the Quality Assurance Program Plan.

#### 3.3.6.2. Standard Evaluation Circuit (SEC)-Appendix 1 of Section A

Documentation is required on the SEC design, including the functionality, its performance limits, and all documentation required for standard design qualification per the TRB.

#### 3.3.6.3. Standard Evaluation Circuit (SEC) Section B

The SEC design and construction baseline form (i.e., DESC EQM-42) shall be included in the manufacturers program plan and maintained under document control. A manufacturer shall have a Standard Evaluation Circuit (SEC) for each technology to be certified. The SEC may be designed solely for its role as a qualification and reliability monitoring vehicle or it may be a product meant for system use.

For initial certification, a sufficient number of SEC devices randomly chosen and evenly distributed from wafers from three homogeneous wafer lots passing PM tests and screened in the technology to be qualified at the fabrication facility to be qualified shall be evaluated for surrogate feasibility. The number of SEC device failures will serve as a qualification benchmark for the technology. Failure Analysis (FA) shall be done on all failed parts and action taken to correct any problems found. The SEC reliability data, including failure analysis results, shall be available for review by the Qualifying Activity.

The TRB shall determine the tests to be accomplished on the TCV, SEC, and PM and submit to the Qualifying Activity a test plan with parametric limits and accept/reject criteria.

The manufacturer shall demonstrate the capability of the assembly and package processes by qualifying the package to be used to house the SEC chip. The test results of the SEC package qualification shall be submitted to the Qualifying Activity as part of the Certification procedure.

#### 3.3.6.4. Standard Evaluation Circuit (SEC)-Appendix 1 of Section B

The Standard Evaluation Circuit (SEC) shall, as a minimum, monitor the long term reliability parameters of the wafer fabrication facility.

When radiation hardness is a requirement of the technology, the SEC shall be used to certify, qualify, and monitor the radiation hardness of a specific fabrication technology in a specific fabrication facility. The SEC

shall be designed so it can be used to assess and monitor the radiation hardness of the technology

#### 3.3.7. Quarterly Report

A Quarterly report is to be issued by the manufacturer's TRB to the Qualifying Activity summarizing all reliability and quality testing results, explaining all modifications to the manufacturing line since last reporting period, and detailing the disposition of all microcircuits affected by any changes or corrective actions to the process.

##### 3.3.7.1. Quarterly Report-Section A

As part of the quarterly status report the TRB should include a summary of results of any catastrophic failures (i.e., shorts or opens measurable or detectable at 25°C) subsequent to burn-in which were analyzed.

##### 3.3.7.2. Quarterly Report-Appendix 1 of Section A

The manufacturer shall submit to the Qualifying Activity in the Quarterly Reports, any deficiencies and corrective actions. The Qualifying Activity may modify the frequency of the self-audit or require additional testing based on the data from the self-audit.

#### 3.4. SUMMARY

The investigation task culminated with the issuance of the 8 Apr 1988 draft document. This document included inputs from the contract team and the Industry Coordinating Working Group (ICWG). In an attempt to include requirements and standards in a single document, a multi-section document was drafted. Section A identified General Requirements; section B included Line Certification Requirements; and section C was Qualification Requirements. Each section included appendices. Section A Appendix 1 was Quality Assurance Program requirements, Appendix 2 was Statistical Process Control Plan requirements, Appendix 3 was Device Specification requirements and Appendix 4 was Statistical Process Control requirements. Section B Appendix 1 was Quality/Reliability Vehicle requirements and Appendix 2 was Audit Checklist

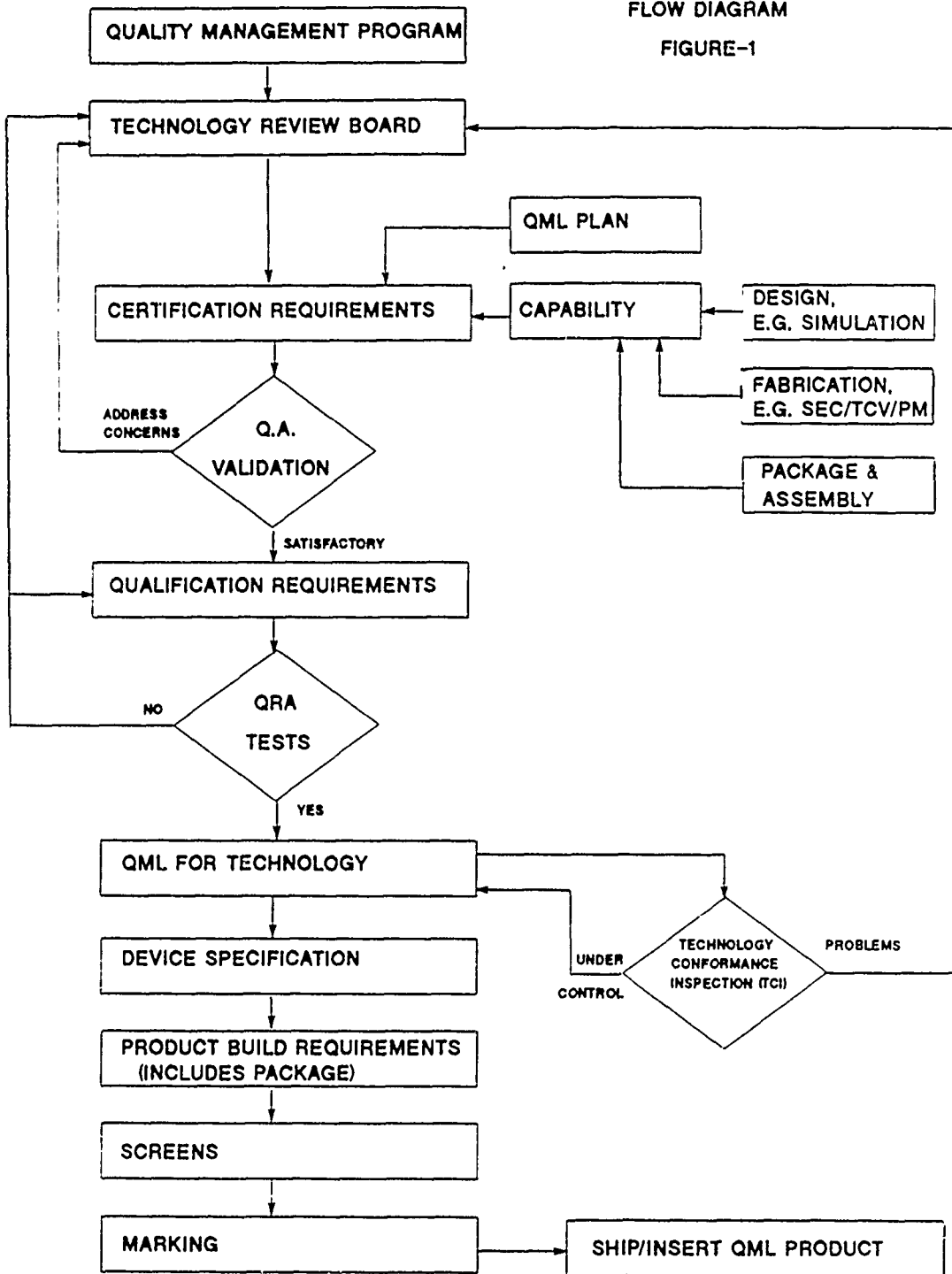
for QML Microcircuit Certification requirements. The final section to the 8 April 1988 draft document was "Method XXXX" which included all testing requirements for qualification and screening.

Key elements that developed during this phase were, Total Quality Management, Technology Review Board, Standard Evaluation Circuit, Parametric Monitor, Technology Control Vehicle, and QML Plan. The goal in establishing this generic qualification procedure document, was to identify those controls and measurements that made sense to industry and DoD without restricting the ability of integrated circuit manufacturers to improve and maintain highly reliable and quality products.

The activity of the investigation task was reported in an interim report and orally at the VHSIC/VLSI Qualification, Reliability and Logistics Workshop, September 1988, in Scottsdale, Arizona.

The draft procedures underwent an extensive review during the next year and from that review the following Generic Qualification Flow Diagram shown in Figure 1 emerged.

GENERIC QUALIFICATION  
FLOW DIAGRAM  
FIGURE-1



#### **4. TASK III - DEMONSTRATION AND GENERAL SUPPORT**

##### **4.1. INTRODUCTION**

For Task III the contract team was required to demonstrate the proposed QML procedures by implementing them on their own VHSIC/VLSI process lines. To accomplish this task alpha sites at GE and AT&T were chosen. In addition to these alpha site demonstrations the contract team would also provide support for beta site demonstrations which would be conducted by companies solicited from the VLSI community at large. The contract team also accumulated a large set of data on state-of-the-art VLSI equipment, software, and techniques for use in preparation of a handbook which could be made available to the industry.

Both GE and AT&T used draft versions of MIL-I-38535 (the QML requirements document). Some differences in requirements occurred as the document and team understanding matured.

##### **4.2. ALPHA SITE DEMONSTRATIONS**

The GE alpha site consisted of the GE design center at Utica, NY. The technology in use was a 1.25 micron CMOS standard cell process which was fabricated, assembled and tested at GE Microelectronics Center (GE-MEC) in Research Triangle Park, NC. GE planned to demonstrate three chips with a complexity of 6,000, 21,000, and 28,000 gates respectively, plus an SEC containing 10,000 gates.

The QML alpha site for AT&T in Allentown, PA involved their Bell Laboratory Design Center, AT&T-ME Mask Facility, MOS V CMOS Clean Room, and the "Just-in-Time" (JIT) Ceramic Assembly and Test Area. A standard evaluation circuit, a technology evaluation vehicle, and three production devices were fabricated in order to demonstrate the generic qualification principle. AT&T formed a TRB which submitted a quality plan in July of 1988 to start the formal process of qualification.

#### 4.2.1. Alpha Site Validation

The certification phase of generic qualification involves a process of validation of the manufacturers capability. The validation process has two parts. In the first part the manufacturer submits documentation to DESC/RADC on his quality programs and process capabilities. After evaluation of the submitted documentation DESC/RADC performs an on-site validation review to provide a final assessment of the manufacturers readiness.

In order to demonstrate the effectiveness of the requirements documented in the draft MIL-I-38535 specification, RADC performed two practice QML validations at the Contractor sites. The first validation demonstration was a full fledged validation of the entire technology flow at AT&T's Allentown, PA facility in November of 1988. The second demonstration concentrated on GE's Design Center located in Utica, NY and was performed in February of 1989.

##### 4.2.1.1. Pre Validation Submittal

In preparation of the trial validation review conducted by Government representatives from RADC and DESC, both AT&T and GE prepared Quality Assurance Program Plans (later called Quality Management Plan) and submitted them to RADC and DESC before the actual validation. In AT&T's case the Quality Assurance Program plan detailed AT&T's proposed QML technology from design through test. GE's plan concentrated on design only. The following paragraphs summarize the actual review conducted at AT&T and GE.

##### 4.2.1.2. Validation Reviews

A validation team consisting of ten representatives from RADC and DESC performed a certification validation audit at AT&T Allentown PA's facilities on 15-18 of November 1988. The purpose of this demonstration was to test out the concepts associated with a QML validation and make changes to the requirements and procedures based on the outcome.

The first day of the trial validation was an intense review of AT&T's Quality program and proposed technology flow. Present from AT&T was management and the Technology Review Board. Discussions and questions

concentrated on AT&T's business plans for the technology, marketing plans, quality management approach (including TQM), technology review board operation and effectiveness, SPC program including goals and monitoring program and change control program. On the technical side discussions centered on contamination control, SEC design and effectiveness, TCV program, and ESD policy. At the end of the meeting RADC and DESC gave AT&T an outbriefing of their findings.

The next three days were spent with RADC and DESC touring the facilities and spot checking various operations. A full day was spent with the design group where questions centered on how AT&T developed and verified their models used in simulation; and checking designs. AT&T presented detail information on how various design, electrical and reliability rules were established, verified and checked. Tours and audits of AT&T fabrication line, JIT assembly line and test areas were conducted on subsequent days. At the end of each day RADC and DESC gave an outbriefing of their findings.

On the final day, a formal outbriefing was given to AT&T management and TRB. Also, AT&T gave RADC and DESC an outbriefing on how they could better organize and perform an audit function. Generally, the validation was an informative exchange of issues related to reliability, quality, management and environmental concerns. Suggestions for improvements included better definition of what should be submitted to the validation team in the Quality Assurance Program plan, smaller audit teams during the facility tours and better organization of questioning during the Design Center Review.

At GE, review of their design center was conducted on 1 Feb 1989. The initial QML validation review was to consist of a review of GE/Utica design and GE/RTP fabrication, assembly and test portions. Only the GE/Utica review was conducted. The following is a summary of the review at GE/Utica.

The Manager of Engineering at GE/Utica presented an Organizational Chart for GE Aerospace down to the ASIC Design Unit level. The manager of ASIC Design, provided a brief summary of the AVLSI 1.25 micron technology and



reviewed the Technology Review Board (TRB) function at GE/Utica and the interface with the GE/RTP TRB.

GE/Utica encouraged the RADC representatives to be open and frank with any issues that were to be addressed during the validation review. At that time RADC presented an overview of the Qualification Procedures activity to date and the intent of the Validation Review.

During the remaining portion of the Validation Review question and answers were exchanged between RADC and GE representative.

- o GE/Utica ASIC Design function deals mainly with internal system requirements and an informal hand-off is made from systems engineering. For QML validation, a documented and TRB approved hand-off of system requirements is required.
- o Since GE/Utica interfaced with GE/RTP for fabrication, design rules and cell library maintenance was handled by GE/RTP. A documented interface between GE/Utica and GE/RTP was required for the validation review. The interface process was electronic but not well documented. GE/Utica's position that GE/RTP would present that documentation during a subsequent validation at GE/RTP still did not demonstrate an "in place" system. Interface responsibility must be shared between design and fabrication functions and validated by both functions.
- o GE/Utica does not have behavioral models but does have structural models which could be converted into VHDL structural models with an implemented translator. GE/Utica is actively pursuing VHDL in the future development of ASIC design. Designer training and VHDL implementation in future CAD tools is part of the on-going effort at GE/Utica. Review of MIL-STD-454, requirement 64, was needed to better understand the VHDL requirement.

#### 4.3. BETA SITE DEMONSTRATIONS

A number of companies, in addition to the alpha site companies, were invited by DOD to participate in the refinement of MIL-I-38535 prior to its formal release. These volunteer participants were helpful in the coordination of the requirements. The beta site companies would be among the first manufacturers to be formally audited to the Qualified Manufacturer's List (QML) requirements defined in MIL-I-38535.

##### 4.3.1. Companies Involved in Beta Sites

Eight companies accepted the beta site invitations and plan to demonstrate compliance to the requirements of MIL-I-38535. These were:

GE Solid State	Findley OH
Harris Semiconductor	Melbourne FL
Intel	Chandler AZ
National Semiconductor	Sunnyvale CA
Texas Instruments	Dallas TX
VLSI Technologies	San Jose CA
LSI Logics	Milpitas CA
IBM	Manassas VA

Since the beta site commitments have been made, GE Solid State at Findley and GE-MEC have been purchased by Harris Semiconductor, making some alpha and beta site schedules in question. Also, Honeywell in Plymouth, MN was added as beta site.

##### 4.3.2. Progress

Most of the beta sites plan to obtain QML status by end of 1990. Final release of MIL-I-38535 is expected by the end of 1989.

#### 4.4. BETA SITE MEETINGS

Throughout the beta site process a series of meetings was held between all beta site companies, DOD representatives, and the alpha site companies to discuss major issues of preliminary versions of MIL-I-38535. Each meeting concentrated on a specific topic related to QML; such as fabrication, design/test, assembly/packaging, screens/QCI/Qualification and Radiation Hardness/Space Quality.

The results of these meetings were integrated in subsequent drafts of MIL-I-38535. A final review of MIL-I-38535 was released for formal coordination in Fall 1989.

#### 4.5. GENERAL SUPPORT

##### 4.5.1. Handbook

As part of the contract a guideline handbook to help the manufacturer in implementation of built-in quality and reliability was developed.

Material for the handbook was solicited from equipment manufacturer and software vendors throughout the microelectronics industry. Nearly 150 data sheets were received in response to this solicitation. The contract team formatted some of the information into handbook form using the format shown in Figure 2. The sample handbook needs to be further expanded to improve its usefulness.

##### 4.5.2. Proposed Test Methods

During the review of existing military documents, several new test methods were identified as necessary to completely test digital devices. There proposed test methods are found in Appendix II and are presently being evaluated by industry and DoD for consideration for inclusion into Mil-Std-883.

VOLUME: FABRICATION

HANDBOOK # 2.A.6

ISSUE DATE: 7/13/89

REVIEW CYCLE: 12 Mo.

REVIEW DATE:

CATEGORY: EQUIPMENT

IDENTIFICATION: SAMCO PDM-303

APPLICATION: PLASMA CVD MULTI-CHAMBER

## DESCRIPTION/COST:

This is a multi-chamber reactor for depositing multi-layer amorphous silicon films with each deposited in individual chamber, dual rack mounted units (1710 x 55 x 1050 and 1730 x 1030 x 1050) and a separate RF power control unit. The reactor has fine sample holders with rotating mark plate. There are three independent reaction (p, n, and i) chambers with a fourth "loading chamber", all enclosed in safe enclosure. The main unit has easy access gas inlets and outlets and a built-in vacuum system with its own vacuum/pressure gauges and gas flow meters.

SAMCO indicates that prices start at \$25,000 and range up to about \$100,000 for a single chamber system, depending on application and options.

## DOCUMENTATION/SUPPORT:

OPTO FILMS, a research laboratory in the United States for SAMCO, provides after sales service, applications advice, user's manuals, installation assistance, and training.

## USERS:

A list of customers is available to potential customers on a case by case basis. The list includes many well-known companies and universities in the United States and Japan.

## USERS:

## COMPANY/CONTACT:

Japan: SAMCO International Inc.

33 Tanakamiya-cho, Takeda, Fushimi-ku  
KYOTO 612 JAPAN

Phone (075) 621-7841

Fax # (075) 621-0936

Telex 5422864 SAMCO-J

USA: Opto Films

532 Wedell Drive, Ste. 5  
Sunnyvale, CA 94089

Phone (415) 734-0459

Fax # (408) 734-0961

## TECHNICAL DATA:

Electrode: Parallel plate

Reactor: 3 chambers (\*2 or 4 chambers), pyrex made (\*quartz or stainless steel)

Substrate: Max 350°C, 160 mm , each unit can be heated

Gas control: Mechanical flow meter (3 units)

RF power supply: 13.56 MHz, 150 W or \*400 W

Sample preparation chamber: Stainless made

Vacuum line: Reactor - oil diffusion pump, PC - rotary pump

Vacuum gauge: Thermocouple gauge, capacitance manometer, ionization gauge

### Optional Accessories:

- o Mass flow controller (in case of adding more than 3 components)
- o Plasma radiation monitor (wave length 200-800 nm)
- o Gas scrubber unit (for SiH<sub>4</sub>, PH<sub>3</sub> and B<sub>2</sub>H<sub>6</sub>)
- o Toxic gas monitor (PH<sub>3</sub>, AsH<sub>3</sub>, H<sub>2</sub>S and etc.)
- o Computer controller

## FEATURES:

- o Deposition of multi-layer amorphous silicon films with each layer deposited in an independent chamber (example: p, i, n layers)
- o Multi-step plasma etching and stripping of semiconductor products
- o Deposition, sputtering, or vacuum evaporation can also be incorporated into the total process using a single multi-chamber system.

Figure 2. Cont'd

## 5. CONCLUSIONS AND RECOMMENDATIONS

### 5.1. CONCLUSIONS

Generic qualification of the manufacture of VHSIC/VLSI microcircuits is a concept whose time has come. From the beginning of the contract, until its completion, the importance of quality management and the need for a "living" document have reverberated throughout industry. The concept of "building in" quality by characterizing and controlling the process was readily agreed upon by both the contract team and the customer. Releases from DoD during the contract period further supported a commitment to total quality management and streamlining the procurement policies within the DoD. With a clear objective set, the real challenge was to provide a well documented policy for the DoD which provided industry a clear concise method for qualifying a manufacturing process from design through final procurement by the DoD. Highlights of how the resulting qualification procedures for VHSIC/VLSI met the goals of the contract are give in the areas of design, fabrication, assembly and test.

#### 5.1.1. Design

The design community is well equipped with CAE and CAD tools to provide verified designs and test criteria to the fabrication, assembly and test processes. The new procedures stress the need of design to interface and maintain ongoing concurrence with these processes. A design methodology may be qualified under the new procedures by including the design function in the manufacturer's overall quality management plan. Although design tools themselves are not qualified, they become part of a qualified process, showing a well documented design flow and control of all steps and tools used within the flow.

#### 5.1.2. Fabrication

Previously qualification of DoD procured microcircuits was only done through qualification testing of parts that were fabricated on a certified line. For generic qualification, the fabrication processes are now able to be qualified with a well documented quality management plan guaranteeing built in quality and reliability. With well defined fabrication processes

using tools such as statistical process control and standard evaluation circuits, the manufacturer's fabrication process can be qualified in conjunction with its approved quality plan. Both high volume and low volume designs benefit with only surrogate devices required for qualification testing. The new qualification document encourages constant improvement in quality and reliability with quarterly status reports to the qualifying activity notifying them of qualification status and proposed changes for improvement.

#### 5.1.3. Assembly and Packaging

Generic qualification of the assembly manufacturing process ensures that quality and reliability is maintained through continuous control of the assembly process flow. Once the quality management plan is in place to show that characterization of the assembly process has been completed and the processes are well documented and under control, the qualifying activity can validate that the assembly process is ready for line qualification. Once the assembly processes are qualified, process monitoring and in-line testing replaces end-of-process testing. The manufacturer uses his own quality management plan to establish the criteria which ensures quality and reliability in the finished product.

Packaging of microcircuits under generic qualification is also enhanced by allowing minimal need to perform qualification testing of parts due to packaging variations. The packages used for generic qualification can be qualified by package technology styles. When new packages are added to the package technology, only those portions of the characterization testing affected need qualification.

#### 5.1.4. Test

Under generic qualification all phases of screens, and technology conformance inspections (TCI) are integrated from design to final test and shipping of microcircuits. Automatic test equipment is identified, and the design function must design in testability, validate the design through simulations and then provide test vectors to screen finished product. Generic qualification also requires documented interfaces between design,

fabrication, assembly and test to ensure first-pass success on designs at the screening and TCI steps. Reliability and quality requirements are built-in throughout the manufacturing cycle as identified in the manufacturer's quality management plan. ESD protection, electromigration concerns and other reliability issues are addressed prior to the beginning of the design.

## 5.2. RECOMMENDATIONS

Generic qualification has provided the means to qualify the manufacture of microcircuits for many of today's DoD needs based on well established criteria such as temperature, electrical and mechanical stress. There is a need to add radiation and space environment stresses to generic qualification capability if all microcircuit applications are to be totally addressed. Additional modeling and test structures should be developed to enhance generic qualification to eliminate end of process testing that is still required for these applications.

The use of multiple design sites for a given technology should be included in generic qualification to give flexibility to those environments where the front-end design is not an integral part of the fabrication, assembly and test functions. Integration of quality management at remote design sites must be addressed to identify requirements for generic qualification.

Package qualification needs to address off-shore and on-shore issues. The more integrated the quality management plan is the better generic qualification is designed to work. Therefore, as in multiple design sites, there is a need to define an acceptable interface at the Technology Review Board (TRB) level between all phases of microcircuit manufacture.

In addition to the generic qualification document, the guidelines document which was started should be further developed to provide a means of informing the microcircuit industry of on going improvements in microcircuit technologies. Both processes and equipment should be included that would further enhance microcircuit quality and reliability.



## Appendix A

### General Specification for Integrated Circuits (Microcircuits) Manufacturing

MIL-I-38535  
18 December 1989

MILITARY SPECIFICATION  
INTEGRATED CIRCUITS (MICROCIRCUITS) MANUFACTURING,  
GENERAL SPECIFICATION FOR

This specification is approved for use by all Departments and Agencies of the Department of Defense.

This specification is intended to support Government microcircuit application and logistic programs. Detailed characteristics of microcircuits needed for a program are to be defined by detail drawings or specifications.

1. SCOPE

1.1 Scope. This specification establishes the general requirements for integrated circuits or microcircuits and the quality and reliability assurance requirements which must be met for their acquisition. Detail requirements, specific characteristics of microcircuits, and other provisions which are sensitive to the particular use intended shall be specified in the device procurement specification. Quality assurance requirements outlined herein are for all microcircuits built on a manufacturing line which is controlled through a manufacturer's quality management (QM) program and has been certified and qualified in accordance with requirements herein. The manufacturing line shall be a stable process flow for all microcircuits. A single level of product assurance (including Radiation Hardness Assurance (RHA)) is provided for in this specification. The certification and qualification sections found herein outline the requirements to be met by a manufacturer to be listed on a Qualified Manufacturer Listing (QML). After listing of a technology flow on a QML, the manufacturer must continually meet or improve the established baseline of certified and qualified procedures, the quality management (QM) program, the technology review board (TRB), the status reporting and quality and reliability assurance requirements for all QML products. This specification also defines the tests which must be performed on each product built. NOTE: This specification requires a manufacturer to establish a baseline. As the technology matures and reliability and quality data are gathered, the manufacturer through the quality management (QM) program and the technology review board (TRB) may modify, substitute or delete tests. Notification of such actions shall be detailed in the status reports submitted to the qualifying activity.

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specifications, standards and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (ODDISS) and supplement thereto, cited in the solicitation.

SPECIFICATIONS

MILITARY

MIL-M-55565 - Microcircuits, Packaging of.

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center (RBE-2), Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

AMSC N/A FSC 5962  
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## MIL-I-38535

### STANDARDS

#### MILITARY

- MIL-STD-100 - Engineering Drawing Practices.
- MIL-STD-129 - Marking for Shipment and Storage.
- MIL-STD-883 - Test Methods and Procedures for Microelectronics.
- MIL-STD-1331 - Parameters to be Controlled for the Specification of Microcircuits.
- MIL-STD-1285 - Marking of Electrical and Electronic parts.
- MIL-STD-1686 - Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices).

### HANDBOOKS

#### MILITARY

- MIL-HDBK-263 - Electrostatic Discharge Control Handbook for Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices).

Unless otherwise indicated, copies of federal and military specifications, standards, and handbooks are available from the Naval Publications and Forms Center, (ATTN: NPODS), 5801 Tabor Avenue, Philadelphia, PA 19120-5099, or telephone (215) 697-2179.)

2.1.2 Other Government documents, drawings, and publications. The following other Government documents, drawings, and publications form a part of this document to the extent specified herein. Unless otherwise specified, the issues are those cited in effect on the date of the solicitation.

- Handbook H4/H8 - Commercial and Government Entity (CAGE) Handbook.
- DESC-EQM-42 - Baseline Sheet for JAN Microcircuits.
- NAVSHIPS 0967-190-4010 - Manufacturer's Designating Symbols.

(Copies of other Government documents required by contractors in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

#### ELECTRONIC INDUSTRIES ASSOCIATION (EIA)

- EIA-STD-RS-471 - Symbol and Label for Electrostatic Sensitive Devices.
- JEDEC Publication 19 - General Standard for Statistical Process Control.
- JEDEC Publication 108 - Distributor Requirements for Handling Electrostatic Discharge Sensitive (ESDS) Devices.
- JEDEC Publication 109 - General Requirements For Distributors of Military Integrated Circuits.

(Application for copies should be addressed to the Electronic Industries Association, 2001 Eye Street, N.W., Washington, DC 20006.)

NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY

Malcolm Baldrige National Quality Award.

(Application for copies should be addressed to Malcolm Baldrige National Quality Award, National Institute of Standards and Technology, Gaithersburg, MD 20899.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

**2.3 Order of precedence.** In the event of conflict between the text of this specification and the references cited herein (except for device procurement specifications), the text of this specification shall take precedence. Nothing in this specification, however, shall supersede applicable laws and regulations unless a specific exemption has been obtained.

**3. REQUIREMENTS**

**3.1 General.** The manufacturer of microcircuits in compliance with this specification shall have and use production and test facilities and a quality management (QM) program to assure successful compliance with the provisions of this specification.

**3.1.1 Reference to applicable device procurement specification.** For purposes of this specification, when the term "as specified" is used without additional reference to a specific location or document, the intended reference shall be to the device procurement specification.

**3.1.2 Conflicting requirements.** In the event of a conflict between the requirements of this specification and other requirements of the device procurement specification, the precedence in which requirements shall govern, in descending order, is as follows:

- a. Applicable device procurement specification.
- b. This specification.
- c. Specifications, standards, and other documents referenced in 2.1.

**3.2 Item requirements.** The individual item requirements for integrated circuits delivered under this specification shall be documented in the device procurement specification prepared in accordance with 3.6 herein. Unless otherwise specified, all devices produced under this specification shall have a temperature range of -55°C to +125°C. However, the standard evaluation circuit (SEC) shall be documented on a device procurement specification and shall have an operating temperature (case or ambient, as specified) range from -55°C to +125°C and any references to minimum or maximum operating temperatures shall refer to the respective lower and upper limits of this range. NOTE: If any of the provisions of this document are violated or not met, total compliance cannot be claimed to this document and devices cannot be provided as QML devices.

**3.2.1 Country of manufacture.** All QML microcircuits shall be manufactured, assembled, and tested within the United States and its territories except as provided by international agreement establishing reciprocal and equivalent government quality control systems and procedures.

**3.3 Classification of requirements.** The requirements of the microcircuits are classified in the generic qualification flow diagram (see figure 1).

**3.3.1 Certification of conformance and acquisition traceability.** Manufacturers or suppliers including distributors who offer QML microcircuits described by this specification shall provide written certification, signed by the corporate officer who has management responsibility for the production of the QML microcircuits, (1) that the QML microcircuits being supplied have been manufactured and tested in accordance with this specification and conform to all of its requirements, (2) that all QML microcircuits are as described on the certificate of conformance which accompanies the shipment, and (3) that dealers and distributors have handled the QML microcircuit in accordance with the requirements of JEDEC Publications 108 and 109. The responsible corporate official may, by documented authorization, designate other responsible individuals to sign the certificate of conformance (such as members of the TRB), but, the responsibility for conformity with the facts shall rest with the responsible corporate officer. The certification shall be confirmed by documentation to the government or to users with government contractors or subcontractors, regardless of whether the QML microcircuits are acquired directly from the manufacturer or from another source such as a distributor. When other sources are involved, their acquisition certification shall be in addition to the certificates of conformance and acquisition traceability provided by the manufacturer and previous distributors. The certificate shall include the following information:

**a. Manufacturer documentation:**

1. Manufacturer's name and address.
2. Customer's or distributor's name and address.
3. Device type.
4. Date code and latest reinspection date, if applicable.
5. Quantity of devices in shipment from manufacturer.
6. Statement certifying QML microcircuit conformance and traceability.
7. Signature and date of transaction.

**b. Distributor documentation for each distributor:**

1. Distributor's name and address.
2. Name and address of customer.
3. Quantity of devices in shipment.
4. Latest reinspection date, if applicable.
5. Certification that this shipment is a part of the shipment covered by the manufacturer's documentation.
6. Signature and date of transaction.

**3.4 Quality management program**

**3.4.1 General.** A quality management program shall be developed and implemented by the manufacturer and documented in the QM plan (see 3.4.3). Also, the manufacturer shall use the questions posed by the Malcolm Baldrige Quality Award as a self-assessment of their quality program and prepare answers to the questions for the year that QML is pursued. The manufacturer shall submit these answers to the qualifying activity before certification is granted. The manufacturer is encouraged to apply for the Malcolm Baldrige National Quality Award within five years of initial request for QML status.

**3.4.2 Technology review board (TRB).** A TRB shall be formed and shall be responsible for development of the QM plan, maintenance of all certified and qualified processes, process change control (see 3.4.4), reliability data analysis, failure analysis, corrective actions, QML microcircuit recall procedures, and qualification status of the technology.

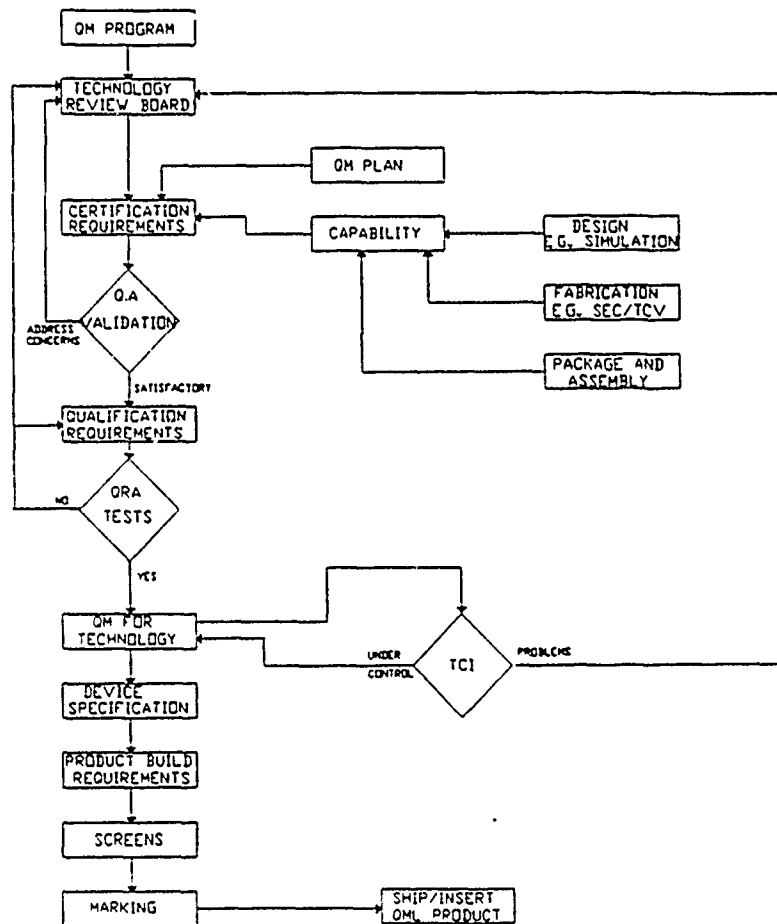


FIGURE 1. Generic qualification flow diagram.

**3.4.2.1 Organizational structure.** The manufacturer's TRB shall consist of, as a minimum, representatives of device design, technology development, wafer fabrication, assembly, testing, and quality assurance organizations. Records shall be maintained of the TRB's membership, deliberations and decisions, and the manufacturer shall submit the names, work addresses, and phone numbers of the members of the TRB to the qualifying activity. Any changes to the TRB membership shall be documented with the qualifying activity. If the change involves the contact person or persons, immediate notification is required.

**3.4.2.2 TRB duties.** The TRB shall keep the qualifying activity updated on the reliability status of QML technology and products. The manufacturer's TRB shall judge the current status of the quality and reliability of its microcircuits by review of the statistical process control (SPC) procedures and QM status of the manufacturer's line, reliability test data (i.e., parametric monitor (PM), technology characterization vehicle (TCV), standard evaluation circuit (SEC) and device), the rate of board assembly failures and field returns, and the failure analysis (FA) results of burn-in failures and board assembly and field returns. The TRB shall maintain records, available for review by the qualifying activity, of the conditions found and the actions taken.

When the reliability data indicates corrective action is required, the TRB shall determine and implement the appropriate action in a timely manner. The SEC and TCV data are to be used as a tool for monitoring the quality and reliability of the manufacturer's line and do not automatically disqualify a manufacturer when trends or limits require corrective action.

When reliability of shipped microcircuits is called into question, the TRB shall provide quick evaluation and corrective action and prompt notification to the qualifying activity to preserve the manufacturer's qualified status and assure that defective product is not shipped.

**3.4.3 Quality management (QM) plan.** The TRB shall oversee and approve the quality management (QM) plan consisting of the following activities and initiatives, as a minimum:

- a. Quality enhancement plan. This plan documents the specific procedures to be followed by the manufacturer to assure quality in the product being produced.
- b. Manufacturing process failure analysis program. This program outlines the self-imposed procedures that a manufacturer takes to test and analyze failed parts from all stages of manufacturing including original equipment manufacturer (OEM) returns, and make corrective actions based on the findings.
- c. Field failure return program. This program establishes the procedures that a manufacturer self-imposes to test and analyze failed parts from the field and implement corrective actions.
- d. Quality improvement plan. This plan defines the self-imposed internal procedures followed by the manufacturer to continuously improve quality and reliability of the processes and the product.
- e. SPC plan. A specific plan defining the manufacturer's goals and plans to impose a SPC program within the manufacturing process to the requirements of JEDEC Publication 19.
- f. Corrective action plan. This plan describes the specific steps followed by the manufacturer to correct any process which is out of control or found to be defective.
- g. Change control program. This program addresses the process by which a manufacturer addresses changes to the technology. Further information of areas to be considered critical for change control are outlined in 3.4.4 herein.

- h. SEC and TCV assessment plan (see 3.5.1.3.2). The frequency, testing methods, and criteria for evaluations of the SEC and/or the TCV are to be determined by the TRB based on the manufacturer's assessment of risk. The manufacturer's SEC and TCV evaluation plan shall be documented.
- i. Certification and qualification plan. The certification and qualification plan shall be to the requirements defined in 3.5 herein including self-audit and corrective actions.

3.4.3.1 Quality management (QM) plan outline. The following shall be addressed in the QM plan. Submittal of the QM plan is required before the validation (certification) meeting. The plan, described in 3.4.3, is included in the outline below.

- a. Index of certified baseline documents.
- b. Conversion of customer requirements.
  - 1. Device specification requirements.
  - 2. Controlled design procedures and tools (established geometric, electrical, and reliability design rules).
  - 3. Mask generation procedure within the controlled design procedures of 2.
  - 4. Wafer fabrication capabilities baselined.
  - 5. Product built in accordance with approved design, mask, fabrication, assembly, and test flows.
  - 6. QML listing coverage.
  - 7. SEC, TCV, and PM programs and test procedures (see 3.4.3h).
  - 8. Incoming inspection and vendor procurement document covering design, mask, fabrication, and assembly.
  - 9. Screening and traveler.
  - 10. Technology conformance inspection (TCI) procedures.
  - 11. Marking.
  - 12. Rework.
- c. Function organization chart (TRB, quality assurance (QA), production, including charters).
- d. Flow charts (design through shipment).
- e. Change control program (see 3.4.3g).
  - 1. Major changes.
  - 2. Required testing.
  - 3. TRB responsibility (e.g., notification policy).
  - 4. TRB MIL-I-38535 program interface for Defense Electronics Supply Center (DESC).
- f. Failure analysis (see 3.4.3b, c, and f).
- g. Self-audit program and audit results.
- h. TRB reporting (to DESC) checklist and procedure.
- i. Yield improvement program (see 3.4.3a and d).
- j. SPC program including in-line process monitors (PM's) (including location and procedure number on applicable flow charts; see 3.4.3e).
- k. Test method suitability including outside lab.



l. Major test methods submitted.

1. Burn-in.
2. Temperature cycle.
3. Fine and gross leak.
4. Particle impact noise detection (PIND).

m. Calibration.

n. Retention of qualification.

o. Training.

p. Cleanliness and atmospheric controls.

q. ESD program.

r. Certification and qualification test plan (see 3.4.3i).

3.4.3.2 Change to the QM plan. After the TRB has approved the QM plan, it shall be kept current and up-to-date and reflect all major changes. This includes updating and keeping current the process flow.

3.4.4 Change control procedures. The following paragraphs outline areas of concern where a change may require action by the manufacturer. All changes to any part of a QML manufacturer's line are to be governed by the manufacturer's TRB and made available to the qualifying activity. All changes shall be documented as to the reason for the change with supporting data taken to support the change, including reliability data. The decision as to the criticality of the change shall be guided by the potential effect of the change on quality, reliability, performance and interchangeability of the resulting microcircuits. For any change that merits consideration for requalification, the TRB shall decide if requalification is needed. Microcircuits shall be shipped following a change only upon approval of the TRB. Deviations to screens and technology conformance inspections (TCI) are allowed but must be justified, documented and submitted to the qualifying activity. Notification of the change shall be made concurrently to the qualifying activity for a period of not less than one year after initial QML listing. Thereafter, notification shall be made in the TRB status reports (see 3.4.5).

3.4.4.1 Design change. Changes in the design methodology to be evaluated by the TRB shall include but not be limited to changes in the following areas:

- a. Technology data base (cell library).
- b. Design flow.
- c. Design system (computer automated design (CAD), design rules).
- d. Software updates.
- e. Model or modeling procedures.
- f. Configuration management.

3.4.4.2 Fabrication change. Changes in the fabrication process to be evaluated by the TRB shall include but not be limited to changes in the following areas:

- a. Fabrication process sequence or process limits.
- b. Fabrication process materials or material specifications, including epitaxial layer thickness.
- c. Photoresistive materials or material specifications.

- d. Doping material source, concentration, or process technique (e.g., ion implantation versus diffusion).
- e. Cross section diffusion profile.
- f. Passivation or glassification material, thickness or technique (including addition or deletion of passivation).
- g. Metallization system (pattern, material, deposition or etching technique, line width or thickness).
- h. Process flow and baseline (DESC-EQM-42 form).
- i. Conductor, resistor or dielectric materials.
- j. Wafer fabrication move from one line or building to another.
- k. Passivation process temperature and time.
- l. Oxidation or diffusion process, oxide composition, oxidation temperature or time.
- m. Sintering or annealing temperature and time.
- n. Standard evaluation circuit (SEC) and how it is tested.
- o. Method of mask making.
- p. Process monitor (PM) and how it is tested.
- q. Wafer acceptance criteria.
- r. Technology characterization vehicle (TCV) and how it is tested.
- s. Sample plans (quantity and acceptance numbers) and lot formation.

3.4.4.3 Assembly change. Changes in the assembly process to be evaluated by the TRB shall include but not be limited to changes in the following areas:

- a. Die attach material, method, or location.
- b. Wire bond method.
- c. Wire material composition and dimensions.
- d. Seal technique (materials or sealing process, gas composition (e.g., for RHA)).
- e. Implementation procedures for internal visual and other test methods.
- f. Assembly flow.
- g. Assembly operation move.
- h. Scribing and die separation method.
- i. Technology conformance inspection (TCI) procedures including manufacturer imposed tests.
- j. Screening tests.

- k. Sample plans (quantity and acceptance numbers) and lot formation.
- l. Die back surface preparation.
- m. Bond pad geometry, spacing, or metallization.

3.4.4.4 Package change. Changes in the package qualification to be evaluated by the TRB shall include, but not be limited to changes in the following areas:

- a. Vendor.
- b. External dimensions.
- c. Cavity dimensions.
- d. Number of leads or terminals.
- e. Lead or terminal dimensions (length times width or diameter).
- f. Lead or terminal base material.
- g. Lead or terminal plating material.
- h. Lead or terminal plating thickness (range of).
- i. Body material.
- j. Body plating material.
- k. Body plating thickness (range of).
- l. Die pad material.
- m. Die pad plating.
- n. Die pad plating thickness (range of).
- o. Lid material.
- p. Lid plating materials (range of).
- q. Lid plating thickness (range of).
- r. Lid seal (preform) material.
- s. Lid glass seal material.
- t. Lead glass seal material.
- u. Lead glass seal diameter (range of).
- v. Leads or terminals spacing.
- w. Leads configuration (e.g.  $\lambda$ , gull wing).
- x. Die size.
- y. Device marking process.

3.4.4.5 Test facility change. Changes in the test facility to be evaluated by the TRB shall include but not be limited to changes in the following areas:

- a. Implementation procedures for internal visual and other test methods.
- b. Testing flow.
- c. Test facility (with laboratory suitability) move from one facility or building to another.
- d. Sample plans (quantity and acceptance numbers) and lot formation.
- e. Test procedures (including test vector generation).

3.4.4.6 Miscellaneous changes. These general concerns need to be addressed by the TRB:

- a. Key managerial (corporate and TRB) changes.
- b. Business plans (mergers, new technologies).
- c. Calibration procedures.

3.4.5 Status report. The manufacturer's TRB shall submit a status report to the qualifying activity describing the health of the QML manufacturer's line including all changes and the criticality of the changes in microcircuit quality, reliability, performance and interchangeability. Support test data shall be retained by the manufacturer. The qualifying activity can request to review the supporting data. The following areas shall be discussed and updated in each status report:

- a. TRB meeting minutes.
- b. Integrated circuits shipped.
- c. Field returns and corrective actions.
- d. SPC program.
- e. SEC and TCV test data summary, including radiation data if applicable.
- f. Design facility.
- g. Fabrication line.
- h. Assembly facility.
- i. Test facility.
- j. Major changes (completed or proposed).
- k. Defect density summary.
- l. Newly qualified packages.

The frequency of the status reports to the qualifying activity shall be determined by the TRB, but shall be as a minimum quarterly for the first year following the attainment of QML status and as a minimum biannually (no further than six months apart) thereafter. If major problems with the technology are encountered, more frequent reports are required to keep the qualifying activity informed of the status. In addition to the above report, the manufacturer shall make a formal presentation yearly to the qualifying activity outlining the status of the technology, products offered and future trends and other strategic business plans of the technology including foreseen changes. At the discretion of the qualifying activity, this presentation may be in lieu of a status report.

**3.4.6 Revalidation reviews.** The frequency of revalidation reviews shall normally not exceed two years.

**3.4.6.1 Drop-in reviews.** The qualifying activity reserves the right to perform drop-in reviews at any time. Minimum notification of a drop-in review will be given to the manufacturer. The drop-in review may involve the entire line or portions of the line.

**3.5 Requirements for qualified manufacturer's listing (QML).** QML involves a two-step procedure of demonstrating compliance to the QML certification requirements (see 3.5.1) and the QML qualification requirements (see 3.5.2). The qualifying activity will determine compliance to the requirements and will list the manufacturer's technology on the QML.

**3.5.1 QML certification requirements.** This section outlines the minimum procedures and requirements for QML certification of a manufacturing line on which integrated circuits are designed and made. The qualifying activity will determine adequacy and compliance to the requirements as specified herein and will report their findings and recommendations to the manufacturer's TRB. Each portion of a QML microcircuit manufacturer's line capability may be demonstrated independently but validation by the qualifying activity will assess a complete technology flow.

For generic qualification procedures, certification shall consist of:

- a. Quality management program documentation.
- b. Process capability demonstration.
- c. Qualifying activity management and technology validation.

**NOTE:** This document sets forth the general requirements for manufacturing microcircuit components. It applies to all technologies and once proven is intended to be used for long periods of time (i.e., years) without modification. Specific technology requirements are spelled out in the detailed guidelines for that technology and will be upgraded periodically to reflect the current state-of-the-art product. The validation process will measure and evaluate the manufacturers' manufacturing process against a baseline for that process. This baseline can include innovative and improved processes that result in a more competitive and higher quality product, provided that the process used to evaluate and document these changes has been reviewed and approved. Changes to the process baseline can be made by the manufacturer's TRB after achieving QML status with documented reliability and quality data. Notification of such change must be given to the qualifying activity in a timely manner (see 3.4.4).

**3.5.1.1 Quality management program documentation.** The manufacturer shall have in place a program to implement quality management (QM) in accordance with the requirements of 3.4 herein. The QM program shall document how a manufacturer intends to provide for continual product quality and reliability improvement. A QM plan (see 3.4.3) detailing the QM program shall reflect a self-audited implemented program and shall be submitted, along with the answers to the Malcolm Baldrige National Quality Award questions, to the qualifying activity before a management and technology validation is scheduled.

3.5.1.1.1 QML certification and qualification test plan (see 3.4.3i). Before a management and technology validation is scheduled, the manufacturer shall submit to the qualifying activity a TRB approved test plan with milestone charts outlining the tests to be used to certify processes and the tests and devices to be used to qualify the certified processes to the requirements of 3.5. The TRB shall determine the tests to be accomplished on the TCV, SEC, and PM and submit to the qualifying activity a test plan with parametric limits and accept and reject criteria. For RHA environments, post irradiated endpoint parameter limits (PIPL) values need to be established for PM (if applicable), SEC, and TCV. Devices which fail during the certification demonstration shall be failure analyzed to determine failure modes and mechanisms and corrective action is required. A test report detailing the test results, failure analysis results, and corrective actions shall be submitted as part of the certification procedure to the qualifying activity.

3.5.1.2 Process interface procedures. The manufacturer shall demonstrate that the interfaces between processes are under control and verification tests are performed. Listed below are examples:

- a. Design to and from fabrication.
- b. Design to and from assembly.
- c. Design to and from package.
- d. Design to and from test.
- e. Design to mask.
- f. Mask to fabrication.
- g. Fabrication to and from assembly.
- h. Fabrication to and from package.
- i. Fabrication to and from test.
- j. Assembly to and from package.
- k. Assembly to and from test.
- l. Package to and from test.

3.5.1.3 Process capability demonstration. As part of certification, the manufacturer shall build devices, perform tests and run software benchmarks necessary to demonstrate that the manufacturer has a comprehension of the capability of the manufacturing process as related to quality, reliability and producibility. The summary of the results of these tests shall be submitted to the qualifying activity before the management and technology validation. These tests shall be designed to be used as a continual check of the process capability as well as an initial demonstration of such capability. The TRB shall determine when such tests need to be performed after initial certification.

For RHA, a radiation hardness assurance capability level (RHACL) must be established for the environments selected by the TRB and demonstrated for a technology at a specified electrical performance. Changes in the RHACL may require reevaluation of these capabilities by the TRB. Listed below are the RHA environments:

- a. Natural:
  - 1. Total dose and time dependent effects for ionizing radiation.
  - 2. Cosmic ray - single event phenomena (SEP): upset, latchup and burnout.

b. **Weapon:**

1. Dose rate: upset, latchup, burnout.
2. Neutrons.
3. Total dose.

3.5.1.3.1 Design. The manufacturer shall demonstrate the process capability for the following areas of design:

- a. Model verification. Provide evidence that all models utilized in the design process are functional, predictable and accurate over the worst case temperature and electrical extremes. Examples of these models are: behavioral, logic, fault, timing, simulation, fabrication, assembly and package. For RHA, provide evidence that models defining device response in radiation environments are functional, predictable and accurate over worst-case temperature and voltage extremes and RHACL.
- b. Layout verification. Demonstrate the capability of the automated or manual procedures routinely used for design, electrical and reliability rule checking to catch all known errors singly and combinationally. These rules cover, as a minimum:
  1. Design rules check (DRC) - geometric and physical.
  2. Electrical rules check (ERC) - shorts and open, connectivity.
  3. Reliability rules - electromigration and current density, IR drops, latchup, single event upset (SEU), hot electrons, ESD, burnout.
- c. Performance verification. The manufacturer shall design a chip or set of chips to assess the process capability to perform routing and to accurately predict post-routing performance. The manufacturer shall demonstrate that the actual measured performance for each function over temperature and voltage falls between the two worst case CAD simulation performance limits. For RHA, post irradiation performance must be demonstrated to fall between the two worst-case CAD simulation performance limits at the RHACL.
- d. Testability and fault coverage verification. The manufacturer shall demonstrate a design style and a design-for-test (DFT) methodology which, in conjunction with demonstrated CAD for test tools, can provide 99 percent or greater fault coverage on a design of reasonable complexity. The manufacturer shall also address his approach for a testability bus, such as joint test action group (JTAG). The manufacturer shall demonstrate the fault coverage measurement (fault simulation, test algorithm analysis, etc.) capability which is used to provide fault coverage statistics of the design that uses the demonstrated design style, DFT method and CAD for test tools. Measurement of fault coverage shall be in accordance with the procedures defined in MIL-STD-883, test method 5012.

Test plans for each of these areas shall be approved by the TRB and submitted as part of the certification test plan (see 3.4.3i). All tests shall be completed, documented and analyzed and a summary submitted to the qualifying activity before the management and technology validation.

3.5.1.3.2 Wafer fabrication. As part of certification, the manufacturer shall establish a specific technology for the wafer fabrication. The technology consists of the fabrication sequence, design rules and electrical characteristics. Demonstration of wafer fabrication capability consists of the following and all supporting documentation and data must be submitted to the qualifying activity before the management and technology validation.

- a. Statistical process control (SPC) and in-process monitoring program. An in-process monitoring system shall be used by the manufacturer to control key processing steps to insure device yield and reliability. This system shall be documented in the quality management plan. The monitoring system can utilize various test structures, methods and measurement techniques. The critical operations to be monitored shall be determined by the manufacturer based on his experience and knowledge of his processes. The resulting data shall be analyzed by appropriate SPC methods (in accordance with the requirements of JEDEC publication 19) to determine control effectiveness. The following list of critical and key processes shall be used as a guideline by the manufacturer:
1. Incoming mask and fabrication process materials.
  2. Equipment used for wafer fabrication.
  3. Doping material concentration.
  4. Cross section diffusion profile, and epitaxial layer.
  5. Passivation or glassification thickness.
  6. Metallization deposition thickness.
  7. Photolithography and etch line width.
  8. Passivation process temperature and time.
  9. Diffusion process temperature and time.
  10. Sintering or annealing temperature and time.
  11. All reliability test data including the SEC.
  12. Mask inspection and defect density data.
  13. Parametric monitor (PM) test data.
  14. Wafer acceptance test.
  15. Technology characterization vehicle (TCV).
  16. Photoreactive processing (including rework procedures).
  18. Ion implant.
  19. Wafer backside preparation.
  20. Wafer probe acceptance criteria.
  21. Rework.
  22. Oxide thickness.
- b. Technology characterization vehicle (TCV) program. The TCV program shall contain, as a minimum, those test structures needed to characterize a technology's susceptibility to intrinsic reliability failure mechanisms such as electromigration, time dependent dielectric breakdown (TDDB) and hot carrier aging. If other wearout mechanisms are discovered as integrated circuit technology continues to mature, test structures for the new wearout mechanisms shall be added to the TCV program. The TCV program will be used for the following purposes: certification of the technology; reliability monitoring; radiation hardness assurance and monitoring, when applicable; change control; and the characterization of fast-test intrinsic reliability structures.
- NOTE: The test structures necessary to monitor intrinsic reliability failure mechanisms do not have to be a single die or location, but can appear on the PM or the SEC or the device itself. The TCV program (see 3.4.3h) shall, however, indicate where the structures are located and how they are tested and analyzed.
- c. TCV certification. For initial certification, sufficient TCV test structures for each wear-out mechanism shall be subjected to accelerated aging experiments. The TCV test structures shall be randomly chosen from and evenly distributed from three homogeneous wafer lots in the technology to be certified in the fabrication facility to be certified. These wafers must have passed the wafer or wafer lot acceptance requirements (see 3.5.1.3.3). The accelerated aging experiments shall produce an estimate of the mean-time-to-failure (MTF) and a distribution of the failure times under worst case operating conditions and circuit layout consistent with the design rules for each wear-out mechanism. From the MTF and distribution of failures a worst case operating lifetime or a worst case failure rate shall be predicted. Test structures shall be from completed wafers which have



been passivated. A summary of the accelerated aging data and analysis shall be available for review by the qualifying activity. The initial certification MTF, failure distribution and acceleration factors shall be used as benchmarks for the technology to which subsequent TCV results will be compared.

All of the TCV test structures must be packageable using the same packaging materials and assembly procedures as standard circuits in the technology. The TCV structures need not use a fully qualified package since qualified packages will tend to have lead counts far in excess of those needed for intrinsic reliability studies. The packaging requirement for the TCV may be waived by the qualifying activity if the manufacturer can supply documentation showing the equivalence of wafer level and packaged accelerated aging results.

An example of the need to package a TCV test structure concerns the hydrogen content of a ceramic package and its effect on hot carrier aging. It is known that hydrogen present in a MOS device can aggravate hot carrier aging. If the passivation layer of the device does not contain enough hydrogen to mask the presence of hydrogen in the ceramic package, the aging results for hot carrier studies can differ substantially for packaged and nonpackaged devices. The minimum requirements for the TCV structures for specific mechanisms are given below.

1. Hot carrier aging. The TCV shall use structures that monitor hot carrier aging applicable to the technology to be used in QML microcircuits. Device degradation is to be characterized in terms of both linear transconductance ( $g_m$ ) and threshold voltage ( $V_T$ ) and the resistance to hot carrier aging is, to be based on whichever parameter experiences the manufacturers' specified degradation limit for the minimum channel length allowed in the technology. A wafer level fast-test screen shall be established for technologies that are susceptible to hot carrier aging. This test shall be part of the wafer acceptance criteria.
  - (a). MOS. The TCV shall have structures to characterize the effects of hot carrier aging as a function of channel length for MOS transistors for each of the nominal threshold voltages used in the technology. Degradation shall be characterizable in terms of  $g_m$  and  $V_T$ .
  - (b). Bipolar. The TCV shall contain structures for characterizing hot carrier aging of diodes in bipolar technologies.
2. Electromigration. The TCV shall contain structures for the worst case characterization of metal electromigration over:
  - (a). Flat surfaces.
  - (b). Worst case noncontact topography.
  - (c). Through contacts between conductive layers.
  - (d). Contacts to the substrate.

The current density and temperature acceleration factors for electromigration shall be determined and a MTF and failure distribution determined for the worst case current, temperature and layout geometry allowed in the technology. From the MTF and failure distribution, a failure rate for electromigration in the technology shall be calculated.

3. Time dependent dielectric breakdown (TDDB) (MOS). The TCV shall contain structures for characterizing TDDB of gate oxides. The structures shall have gate oxide area and perimeter dominated structures. Separate perimeter structures shall be used for the gate ending on a source or drain boundary and where the gate terminates over the transistor to transistor isolation oxide. The electric field and temperature

acceleration factors for TDDB shall be determined and a MTF and failure distribution determined for the worst case voltage conditions and thinnest gate oxide allowed in the technology. From the MTF, a failure rate for TDDB in the technology shall be calculated.

4. Radiation hardness assurance. When radiation hardness is a requirement of the technology, special structures shall be incorporated into the TCV program to characterize the technology's capability for producing radiation hardness assurance devices to the RHACL. Irradiate TCV to RHACL or until failure to determine failure mode and mechanisms. Also, the RHACL and uniformity of the TCV test structures shall be determined for worst case bias conditions and temperature.
  5. TCV fast test structure requirements. The structures to be used for the fast test reliability monitoring of hot electron aging shall be included in the TCV program so that correlations of the fast-test measurements with the accelerated aging results may be made.  
NOTE: It is strongly recommended that fast test intrinsic reliability structures for electromigration and TDDB be included in the TCV program so that correlations can be made with longer term aging experiments. It is likely that these structures will be required for wafer acceptance in the future.
- d. Standard evaluation circuit (SEC). A manufacturer shall have an SEC for the technology to be certified. A manufacturer's SEC shall be used to demonstrate fabrication process reliability for the technology. The SEC design documentation shall include: the design methodology, and the software tools used in the design, the functions it is to perform, its size in terms of utilized transistor or gate count, and simulations of its performance. Documentation procedures for the SEC and standard production devices shall be the same. The SEC may be designed solely for its role as a quality and reliability monitoring vehicle or it may be a product meant for system use. Any SEC, whether specifically designed or a standard product, must exercise the worst-case design rules. For RHA environment, the SEC shall utilize all relevant radiation hardness assurance design rules and shall be used to demonstrate the specified level of performance at the RHACL. The SEC shall be compliant with the following requirements:
1. Complexity. The complexity of the SEC microcircuit shall contain, as a minimum, one half the number of transistors expected to be used in the largest microcircuit to be built on the QML line.
  2. Functionality. The SEC shall contain fully functional circuits capable of being tested, and screened in a manner identical to the QML microcircuits.
  3. Design. The SEC shall be designed to stress all minimum geometric and electrical design rules. The electrical stress requirements for the transistors and interconnects on the SEC shall be worst case conditions. The architecture of the SEC shall be designed so that failures can be easily diagnosed.
  4. Fabrication. The SEC shall be processed on a wafer fabrication line which is intended to be or already is a certified QML line.
  5. Packaging. The SEC shall be packaged in a package qualified in accordance with requirements in 3.5.1.3.5 herein.
  6. Radiation hardness assurance. When radiation hardness assurance is a requirement of the technology, the SEC shall be used to certify and monitor the RHACL of a specific fabrication technology in a specific fabrication facility. The SEC shall be designed so it can be used to assess and monitor the radiation hardness of the fabrication process.

For initial certification, a sufficient number of SEC devices is required, from wafers passing the wafer screen requirements of 3.5.1.3.3 herein, and randomly chosen and evenly distributed from three wafer lots and screened to requirements of 4.3 herein in the technology to be qualified on the fabrication facility to be qualified. The number of SEC device failures will serve as a qualification benchmark for the technology. Failure analysis (FA) shall be done on all failed SECs and action taken to correct any problems found. The SEC reliability data, including failure analysis results, shall be available for review by the qualifying activity. For RHA environments, irradiate SEC to demonstrate RHACL.

- e. Parametric monitor (PM). The manufacturer shall have parametric monitors to be used for measuring electrical characteristics of each wafer type in a specified technology. The PM test structures can be incorporated into the grid (kerf), within a device chip, as a dedicated drop-in die or any combination thereof. Location of the PM test structures shall be optimally positioned to allow for the determination of the uniformity across the wafer. A suggested location scheme is one near the wafer center and one in each of the four quadrants of the wafer, at least 2/3 of a radius away from the wafer center.

The manufacturer's TRB shall establish and document reject limits and procedures for parametric measurements including which parameters will be monitored routinely and which will be included in the SPC program. Documentation of the PM shall also include PM test structure design, test procedure, (including electrical measurement at temperature and the relationship between the measured limits and those determined in the manufacturer's circuit simulations), design rules and process rules. Alternate measurement techniques, such as in-line monitors, are acceptable if properly documented. The following parameters are to be used as a guideline by the manufacturer's TRB in formulating the PM.

1. General electrical parameters.

- (a). Sheet resistance: Structures shall be included to measure the sheet resistance of all conducting layers.
- (b). Junction breakdown: Structures shall be included to measure junction breakdown voltages for all diffusions.
- (c). Contact resistance: Structures shall be included to measure contact resistance of all interlevel contacts.
- (d). Radiation hardness assurance: When radiation hardness assurance is a requirement of the QML line, special structures shall be incorporated into the PM to evaluate the technology's radiation hardness. (See 3.5.1.3.2.c.4).
- (e). Ionic contamination and minority carrier life time: Structures shall be included to measure ionic contamination, such as sodium, in the gate, field, and intermetal dielectrics and minority carrier life time.

2. MOS parameters.

- (a). Gate oxide thickness: Structures shall be included to measure gate oxide thickness for both n and p gate oxides as applicable.

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- (b). MOS transistor parameters: A minimum set of test transistors shall be included for the measurement of transistor parameters. The minimum transistor set shall include a large geometry transistor of sufficient size that short channel and narrow width effects are negligible, and transistors that can separately demonstrate the maximum short channel effects and narrow width effects allowed by the geometric design rules. Both "N" and "P" transistors shall be included for a CMOS technology. If there is more than one nominal threshold voltage for either the "N" or "P" transistor type the minimum set shall be included for each threshold. The transistor parameters to be measured are given below:

- (1). Threshold voltage: The linear threshold voltage for each transistor in the minimum set of transistors shall be measured.
- (2). Linear transconductance: The linear transconductance, (gm), for the full minimum set of transistors shall be measured.
- (3). Effective channel length: The effective channel length for the minimum channel length of each transistor type shall be measured.
- (4).  $I_{on}$ :  $I_{on}$  for each transistor in the set.
- (5).  $I_{off}$ :  $I_{off}$  for each transistor in the set.
- (6). Propagation delay: A test structure shall be available in the form of a functional circuit from which propagation delay information can be measured at room temperature.
- (7). Field leakage: Field transistor leakage for the minimum spaced adjacent transistors at the maximum allowed voltage shall be measured.

3. Bipolar parameters. Care should be taken in the manner and sequence in which all breakdown voltage and current measurements are taken so as to not permanently alter the device for other measurements.

- (a). Sheet resistance: Structures shall be included which can be used to measure sheet resistance of all doped regions, (e.g., emitter, buried collector.)
- (b). Schottky diode parameters: The following measurements shall be made on Schottky diodes representative of the size used in the technology:
  - (1). Reverse leakage: The reverse leakage current  $I_r$  shall be measured at a specified reverse voltage.
  - (2). Reverse breakdown: The reverse breakdown voltage,  $BV$ , shall be measured at a specified current.
  - (3). Forward voltage: The forward turn-on voltage,  $V_f$ , shall be measured at a specified current.

(c). **Bipolar transistor parameters:** The following measurements shall be made on bipolar transistors representative of the size and type used in the technology. The types shall include NPN, Schottky clamped NPN, vertical PNP, and lateral PNP transistors as applicable.

- (1). **Transistor gain:** The common emitter current DC gain, ( $H_{fe}$ ), shall be measured on all representative transistors at 3 decades of collector current, the center of which is at the rated current of the device.
- (2). **Leakage currents:** The leakage currents  $I_{CEO}$ ,  $I_{CBO}$ , and  $I_{EBO}$  shall be measured on all representative transistors at a specified voltage.
- (3). **Breakdown voltages:** The breakdown voltages  $BV_{EBO}$ ,  $BV_{CBO}$ , and  $BV_{CEO}$  shall be measured on all representative transistors at specified currents.
- (4). **Forward voltages:** The forward voltages  $V_{BEQ}$  and  $V_{BCQ}$  shall be measured on all representative transistors at the rated currents.
- (5). **Propagation delay:** A test structure shall be available in the form of a functional circuit from which propagation delay information can be measured at room temperature.

(d). **Isolation leakage:** The isolation leakage current  $I_i$  between minimum spaced adjacent transistor collectors shall be measured at a specified voltage.

4. **Radiation hardness assurance.** When radiation hardness assurance is a requirement of the technology, the PM shall include test structures which address the following RHA concerns when specified:

- a. Latchup (worst-case reflecting the combination of device geometries and layout spacing most likely to produce latchup).
- b. Dose rate.
- c. Single event phenomena (SEP).
- d. Burnout.
- e. Total dose.
- f. Neutron.

5. **Fast-test reliability structures.** Fast test reliability structures are structures meant to evaluate, within a few seconds of testing, a particular known reliability failure mechanism to insure that the processing which an individual wafer received is consistent with the reliability goals of the technology. The fast-test structures are in general new and, with the exception of hot carrier aging structures, are not sufficiently mature. Development work on them is intense however, and it is intended that these structures when mature, will become a mandatory part of the PM. For this reason it has been decided to include information regarding fast-test reliability structures in the following paragraphs. Documentation shall be available which shows the correlation between fast-tests and the results of the more traditional accelerated aging tests performed on the TCV.

- (a). **Hot carrier aging:** A fast-test structure shall be included to evaluate the susceptibility of MOS transistors to hot electron aging. This structure may be one of the PM test transistors.
- (b). **Electromigration:** Worst-case design rule fast-test structures shall be included to evaluate the susceptibility of each metal level and the associated contacts to electromigration.

- (c). Time dependent dielectric breakdown (TDOB): Fast test structures shall be included that can evaluate the long term reliability of gate oxides.

**3.5.1.3.3 Wafer acceptance plan.** The TRB shall develop and demonstrate a wafer acceptance plan based on electrical and radiation (if applicable) measurement of PM's. This plan shall utilize the PM and should include visual criteria, if applicable. In addition, this plan shall address the concerns detailed in MIL-STD-883, test method 2018 (e.g. metallization, step coverage). The use of test method 2018 is encouraged, however alternate procedures utilizing PM's and in-line monitors are accepted if approved during validation. PM data shall be recorded and made available for review. This plan can be either a wafer by wafer acceptance plan or a wafer lot acceptance plan, but must address the following concerns:

- a. Small lots.
- b. Large lots.
- c. Specialty lots.
- d. RHA lots.

NOTE: PM's shall be used to determine wafer and wafer lot uniformity and latchup immunity (when specified). Further testing of the actual device to table VII may be required. As an option to actual device testing, after initial establishment of device specification and device PIPL, the following procedures are presented for the identified and specified radiation environments:

1. Latchup - Utilize worst-case latchup structure to assess latchup threshold at maximum temperature. The holding voltage must be greater than the PIPL. Recommended sampling(accept) criteria: 5(0).
2. SEP - Utilize SEP structures (e.g., cross-coupling resistors to memory cells) to assure critical parameters agree with established PIPL values. Also, for silicon-on-sapphire (SOS) and silicon-on-indium (SOI) technologies assure substrate and epi-layer do not exceed limits. Recommended sampling(accept) criteria: 5(0).
3. Dose rate - Utilize structures to ensure rail span collapse does not cause upset and/or burnout or that metallization resistivity, contact resistance via resistance, epi and substrate resistivity limits are not exceeded. Recommended sampling(accept) criteria: 5(0).

**3.5.1.3.4 Electrostatic discharge sensitivity (ESD).** The manufacture shall provide evidence demonstrating the electrostatic discharge sensitivity of the process using MIL-STD-883, test method 3015. Where input and/or output buffers are utilized the electrostatic discharge sensitivity of these buffers must be evaluated.

**3.5.1.3.5 Assembly and packaging.** The manufacturer shall demonstrate the capability of the assembly and package processes by certifying the SEC package to the package certification procedures described in 3.5.1.3.6. The test results of the SEC package qualifications shall be submitted to the qualifying activity as part of the certification procedure.

- a. **Statistical process control (SPC) and in-process monitoring program.** A process monitoring system shall be used by a manufacturer to control key processing steps to insure product yield and reliability. This system shall be documented in the QM program plan. The monitoring system can utilize various test chips, methods and measurement techniques. The critical operations to be monitored shall be determined by the manufacturer based on his experience and knowledge of his processes. The resulting data shall be analyzed by appropriate

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SPC methods to determine control effectiveness. The following list of critical and key processes shall be used as a guideline by the manufacturer:

1. Incoming assembly process materials.
2. Incoming package acceptance.
3. Equipment used for assembly.
4. Wafer acceptance criteria.
5. Die attach.
6. Chip to package interconnect (wire bond, tab, flip chip).
7. Package seal.
8. Marking.
9. Rework.
10. Lead trim, form and final finish.
11. Atmosphere and cleanliness control.

- b. Assembly processes. The manufacturer shall list the assembly processes (die-attachment, wire bonding, seal and code marking) that is expected to be listed on the QML, and shall qualify those processes by testing of fully assembled packages in accordance with the tests in table I. Sample sizes shall be determined by the TRB.
- c. Internal water vapor content. The manufacturer shall demonstrate and document on a representative package, die attach and device (preferably the SEC), the capability to control internal moisture content of a hermetically sealed device to below 5,000 ppm at 100°C in accordance with MIL-STD-883, test method 1018.

TABLE I. Assembly processes testing.

Group number	Test	MIL-STD-883 test method and condition
1	Thermal shock (100 cycles) End-point electricals Visual inspection Die shear	1011, condition C  2010 die-mounting, die cracks 2019
2	Thermal shock (100 cycles) Visual inspection Bond strength	1011, condition C 2010, wire bonding 2011
3	Mechanical shock Variable frequency vibration Constant acceleration Fine and gross leak Visual inspection End-point electricals	2002, condition B 2007, condition A 2001 1014 Magnification of 20X
4	Internal water vapor (5,000 ppm maximum at 100°C)	1018
5	Moisture resistance Temperature cycling (100 cycles) Fine and gross leak	1004, no bias 1010, condition C 1014
6	Lid torque	2024
	Resistance to solvents	2015

**3.5.1.3.6 Packaging requirements.** All packages used for QML microcircuits shall meet the design requirements and performance characteristics herein. In addition, the processes used for the package assembly of QML microcircuits shall meet all the testing requirements of 3.5.1.3.5 herein.

**3.5.1.3.6.1 Package design and characterization.** Characterization may be performed by the microcircuit manufacturer, by an external laboratory or by the package supplier. In any case, the manufacturer is responsible to maintain documented validation of all characterization methods used, including all supporting data.

- a. **Thermal characterization.** The value of the thermal resistance with free convection and forced cooling air shall be available for all packages used in the manufacture of QML parts. This value may be obtained by direct or indirect measurements, or by simulation tools or calculations. Test method 1012 of MIL-STD-883, may be used for this calculation. If the thermal resistance is obtained by a calculation or simulation tool, this procedure shall be certified. To certify such a method of theoretical estimation, the manufacturer must demonstrate a correlation between the theoretically estimated value and the actual measured value for at least one package of the same style with equal or greater pin count. If a major change, as determined by the TRB, is made to the estimation method, the method shall be certified in accordance with the above procedure.
- b. **Electrical characterization.**
  1. **Ground and power supply impedance.** Packages used in the manufacture of QML microcircuits shall be minimal contributors to ground and power supply noises. The above requirement can be met either through the use of documented package design rules or through testing of the packages, either individually or by similarity, in accordance with test method 3019 of MIL-STD-883.
  2. **Cross-coupling effects.** Cross-coupling of wideband digital signals and noise between pins in packages used for digital QML microcircuits shall be minimized. The above requirement can be met either through the use of documented package design rules or through testing the packages, either individually or by similarity, in accordance with test methods 3017 and 3018 of MIL-STD-883.
  3. **High voltage effects.** The voltage applied to a QML package shall not produce a surface or bulk leakage between adjacent package conductors (including leads or terminals). The above requirement can be met either through the use of documented high voltage package design rules aimed at minimizing bulk or surface leakage, or through testing of the high voltage packages, either individually or by similarity, in accordance with test method 1003 of MIL-STD-883.

**3.5.1.3.6.2 Package procurement requirements.** All packages shall be certified. If a package vendor certification program is used by the manufacturer, it shall be documented and contain as a minimum:

- a. A description of the vendor quality control plan with status update reports as required by the TRB.
- b. A Certificate of Compliance form approved by the TRB as part of incoming material inspection and control.
- c. A description of the procedure used by the vendor for notification of changes in materials or processes.
- d. A package quality control procedure that can be shared or performed by either the vendor or the semiconductor manufacturer.



3.5.1.3.6.3 Package technology styles. All packages used by the semiconductor manufacturer for producing QML parts can be listed by package technology style. A manufacturer can qualify a group of packages within a style with a plan validated by the qualifying activity. A listing of some styles presently available follows:

- a. Dual-in-line package (DIP).
- b. Multiple-in-line package (MIP).
- c. Pin grid array (PGA).
- d. Pad grid array (PAGA).
- e. Flat packs (FP).
- f. Leaded chip carrier.
- g. Leadless chip carrier (LCC).
- h. Metal cans (TO).
- i. Quad package (Qb).
- j. Small outline package (SO).

Table II below outlines minimum tests which shall be addressed on a package technology style in order to characterize them.

TABLE II. Package technology style characterization testing.

Subgroup	MIL-STD-887 test method and conditions
1	2016 - Physical dimensions
2	1011 - Thermal shock, 15 cycles, condition C 2004 - Lead integrity, condition 82 or D 1014 - Seal, fine and gross leak
3	2003 - Solderability (245°C ±5°C)
4	1004 - Moisture resistance, no bias
5	1009 - Salt atmosphere

3.5.1.4 Management and technology validation. The following paragraphs address management and technology validation requirements. The validation by the qualifying activity will include, as a minimum; the following applicable areas of the manufacturer's facility: management quality assurance, design, mask, wafer fabrication, assembly and package, and electrical test. This validation procedure will involve a review of the manufacturer's QM plan and an on-site visit of the manufacturer's facility.

3.5.1.4.1 On-site validation. Manufacturer shall make available to the qualifying activity all data needed to support QM policy and procedures. Qualifying activity access to manufacturing and testing facilities and operators will be required.

3.5.1.4.2 Management validation. The manufacturer's quality management program shall be reviewed, as a minimum, in the areas as listed below. The quality assurance program shall be made evident by a method of self-imposed audits by the manufacturer. Also reviewed at this time, are the answers submitted by the manufacturer to the Malcolm Baldrige National Quality Award (see 3.4.1).

- a. Technology documentation.
- b. Design, fabrication, assembly and testing instructions.
- c. Personnel training.
- d. Procurement control.
- e. Inspection of utilities and work in progress.

- f. SPC and in-process control.
- g. Equipment maintenance and calibration.
- h. Failure and defect analysis and data feedback.
- i. Handling and storage.
- j. Technology review board - authority, responsibilities, duties.
- k. Traceability procedures.
- l. Business plans.

3.5.1.4.3 Technology validation. The manufacturer's technology flow shall be reviewed as an entity for compliance. Detailed information of what the qualifying activity will want to discuss during the validation can be found in the self-audit guideline list (available from the qualifying activity when QML validation is requested) and Validation Procedural Guide (available from the qualifying activity). Some critical areas which will be reviewed by the qualifying activity during the validation are:

- a. Design center procedures.
- b. Design review procedures.
- c. Model verification.
- d. Software configuration and configuration management.
- e. Testability procedures and policies (e.g., JTAG).
- f. Archival system (e.g., VHSLC hardware description language (VHDL)).
- g. Mask inspection procedures.
- h. TCV, SEC, PM tests and data.
- i. Fabrication rework procedures.
- j. SPC program (all areas).
- k. Design rule documentation.
- l. Clean room procedures.
- m. Wafer traceability.
- n. Assembly rework procedure.
- o. Die attach procedures.
- p. Wire bonding.
- q. Device traceability and travelers.
- r. Lot formation (wafer, device and inspection).
- s. Assembly area environmental control.
- t. Internal moisture vapor control program.
- u. ESD control and testing.
- v. Visual inspection.
- w. Human contamination prevention procedures.
- x. Equipment calibration and maintenance.
- y. Training policy and procedures.
- z. Electrical test procedures.
- aa. Screening procedure.
- bb. Technology conformance inspection (TCI) procedures.

3.5.1.4.4 Deficiencies and concerns. Deficiencies and concerns shall be noted by the validation team during an exit critique and will be followed up with a written report. The microcircuit manufacturer shall not receive a letter of certification until all certification requirements are met.

3.5.1.5 Letter of certification. After validation, the qualifying activity shall issue a letter of certification to the manufacturer. The manufacturer shall begin qualification within six months.

### 3.5.2 Qualification requirements for QML

3.5.2.1 QML qualification requirements. This section establishes general requirements applicable to initial qualification testing. Qualification testing shall be performed on two complex microcircuit designs (hereafter designated demonstration vehicles), which have been screened to the requirements of 4.3 herein. The SEC does not qualify as a demonstration vehicle.

**3.5.2.1.1 Qualification eligibility.** Design, wafer fabrication, assembly, and qualification testing of the demonstration vehicles may begin before certification is granted. However, if deficiencies and concerns found during the validation required changes to the process flows, the design, wafer fabrication, assembly and testing must be redone on the new process flows. In all cases, start of the qualification testing of the two demonstration vehicles shall begin no later than six months after the letter of certification is received in order to retain the manufacturer's initial certification. Completion should be achieved in a timely manner or recertification may be necessary.

**3.5.2.1.2 Demonstration vehicles.** The manufacturer shall produce, on the certified manufacturing line, two demonstration vehicles, (the SEC is excluded) as documented in the qualification plan submitted during the certification process. The demonstration vehicles shall be of such complexity as to be representative of the microcircuits to be supplied by the manufacturer. Each demonstration vehicle shall operate and perform in compliance with the device procurement specification (which must be submitted to the qualifying activity) and shall be packaged in packages which have been tested to 3.5.1.3.6 prior to use for qualification.

**3.5.2.2 Qualification test plan.** The manufacturer shall present a qualification test plan as part of the certification information (see 3.5.1.1.1), which details the test flow, test limits, test data to be measured, recorded and analyzed, test sampling techniques, and traceability records. The test plan shall detail materials, manufacturing construction techniques (including design CAD tools), and testing and reporting techniques and shall be submitted to the qualifying activity at the time of certification. The test plan shall include traceability documentation, milestone charts and the proposed demonstration vehicle descriptions. All test limits shall be in accordance with the requirements of this document. All demonstration vehicles (see 3.5.2.1.2) must be screened to requirements of 4.3 and tested in accordance with tables III, IV, V, VI, and VII (if applicable) or tested to a qualifying activity approved manufacturer plan.

**3.5.2.3 Qualification test report.** The TRB shall present to the qualifying activity a comprehensive analysis of the qualification data. The aim of this analysis is to show that all process variables are under control and repeatable within the certified technology and that TCV, SEC, and PM data monitoring is adequate and correlatable to the process. All improvements resulting from qualification testing shall be presented to the qualifying activity. The following data shall be retained by the manufacturer to support the results:

- a. Simulation results from the design process.
- b. PM test data.
- c. Results of each subgroup test conducted, both initial and any resubmissions.
- d. Number of devices tested and rejected.
- e. Failure mode and mechanism for each rejected device.
- f. Read and record variable data on all specified electrical parameter measurements.
- g. Specified electrical tests from a serialized, random sample (minimum of 22 devices) may be used to satisfy this requirement. The manufacturer may submit variables data in histogram format giving mean, and standard deviation or equivalent for passing microcircuits.
- h. Where delta limits are specified, variable data, identified to the microcircuit serial number, shall be provided for initial and final measurements.
- i. For physical dimensions, the actual dimension measurements on three randomly selected microcircuits, except where verification of dimensions by calibrated gauges, overlays, or other comparative dimensions verification devices is allowed.

- j. For bond strength testing, the forces at the time of failure and the failure category, or the minimum and maximum reading of the microcircuits if no failures occurs.
- k. For die shear strength testing, the forces at the time of the failure and the failure category, or the die shear reading if no separation occurs.
- l. A copy of the test data on nondestructive bond pull testing as required by test method 2023 of MIL-STD-883.
- m. For total dose and neutron radiation, pre and post test end-point electrical parameters and test conditions (if applicable).
- n. For lid torque strength testing, the forces at the time of failure or the actual torque if no separation occurs.
- o. For internal water vapor content readings, report all gases found.

3.5.2.3.1 Qualification test failures. If any particular testing results are not successful, the manufacturer shall perform failure analysis and take necessary corrective action. The manufacturer shall notify the qualifying activity of any decision not to pursue qualification of any material or manufacturing construction technique previously certified. After corrective actions have been implemented, qualification testing shall restart.

3.5.2.4 QML listing. A certificate of qualification will be issued upon successful completion of all qualification tests on the two demonstration vehicles and the acceptance of the qualification documentation by the qualifying activity. Issuance of the certificate of qualification will coincide with listing of the manufacturing line on the QML.

3.5.2.4.1 Maintenance and retention of QML. In order to sustain qualification status after initial qualification, the manufacturer shall fabricate and perform qualification testing on the selected SEC and TCV, as defined in the QM plan. Retention of QML status shall also be compliant to 3.5.2.4.3.

3.5.2.4.2 QML line shutdown. The QML line may be shutdown only for preventive maintenance or corrective action purposes. If at any time, there is a shortage of QML microcircuit designs available for manufacture on the QML line, the SEC and PM as defined herein (or equivalent product) shall be continuously produced and tested. The TRB shall determine intervals to assure that a controlled process is still able to produce QML microcircuits when required. Failure to keep the QML line operating during production lulls, is grounds for QML removal by the qualifying activity.

3.5.2.4.3 QML removal. The manufacturer may be removed from the QML by the qualifying activity for any of the reasons listed below.

- a. The manufacturer's QML product does not meet the quality, reliability or performance requirements of this specification and the manufacturer is unable to implement corrective action plan as defined in accordance with this document.
- b. The QML microcircuit offered under contract does not meet the device procurement specification requirements specified herein.
- c. The manufacturer has terminated the QML technology which was qualified.
- d. The manufacturer requests that his company's name be removed from the QML.
- e. One or more of the conditions under which certification and qualification was granted have been violated.
- f. The manufacturer has failed to notify the qualifying activity of change in procedures, processes, etc., in accordance with 3.4.4.

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- g. The manufacturer's name appears on the "Consolidated List Of Debarred, Ineligible, and Suspended Contractors."
- h. The manufacturer has not complied with the requirement for retention of qualification, as stated in 3.5.2.4.1.
- i. The manufacturer has published that his company is the only one qualified to make the QML microcircuit or that the qualifying activity has endorsed his company.
- j. The manufacturer has failed to provide a certified statement, when QML microcircuits are supplied under contract for direct or indirect government use, that such QML microcircuits have been tested to and met all the requirements of this document.

**3.6 Device procurement specification.** Appendix A details the format and data requirements to be submitted with any device procured under MIL-I-38535. The specific requirements required for each device is outlined in appendix A, however, other requirements may be necessary for a given technology, product or special conditions. This specification must be negotiated between vendor and customer before a product build can occur (especially in the Application Specific Integrated Circuit (ASIC) environment). This format follows the Standardized Military Drawing (SMD), in accordance with MIL-STD-100.

**3.7 Marking of QML microcircuits.** Marking of QML microcircuits shall be in accordance with the following requirements and the identification and marking provisions of the device procurement specification. All marking flows shall be certified and qualified. The marking shall be legible, complete and shall meet the resistance to solvents requirements of test method 2015 of MIL-STD-883. The following marking shall be placed on each microcircuit:

**3.7.1 Index point.** The index point, tab or other marking indicating the starting point for numbering of leads or for mechanical orientation shall be as specified in the device specification and shall be designed so that it is visible from above when the microcircuit is installed in its normal mounting configuration. The outline of equilateral triangle(s), which may be used as an electrostatic identifier (see 3.7.7.2) may also be used as the pin 1 identifier.

**3.7.2 PIN.** Each SMD microcircuit shall be marked with the complete part or identifying number (PIN). The number sequence for MIL-I-38535 is 5962-XXXXXZZQYY, where:

5962	-	XXXXX	ZZ	-	Q	Y	Y
Federal stock class designator	RHA designator (3.7.2.1)		Device type no.		QML Device class designator	Case outline (3.7.2.2)	Lead finish designator (3.7.2.3)
Drawing number							

**3.7.2.1 RHA designator.** A "-" indicates no radiation hardness assurance. An "\*" indicates that RHA environment is specified in the device procurement specification.

**3.7.2.2 Case outline.** The case outline shall be designated by a single letter assigned to each outline within each device procurement specification.

**3.7.2.3 Lead finish.** The lead finish shall be designated by a single letter as follows:

Finish letter	Process
A	Hot solder dip
B	Tin plate
C	Gold plate
X	Either A, B, or C (mark on specification only)

**3.7.3 QML certification mark.** All microcircuits acquired to and meeting the requirements of this specification and the applicable device procurement specification, and which are approved for listing on the QML shall bear the "QML" certification mark (if manufactured in the United States).

**3.7.4 Manufacturer's identification.** Microcircuits shall be marked with the name or trademark of the manufacturer. The identification of the equipment manufacturer may appear on the microcircuit only if the equipment manufacturer is also the microcircuit manufacturer. The microcircuit manufacturer's designating symbol or CAGE code number shall be as listed on NAVSHIPS 0967-190-4010 or cataloging Handbook H4/H3. The designating symbol shall be used only by the manufacturer to whom it has been assigned and only on those devices manufactured at that manufacturer's plant. In the case of small microcircuits, the manufacturer's designating symbol may be abbreviated by omitting the first "C" in the series of letters.

**3.7.5 Country of origin.** The phrase "Made in U.S.A." shall be marked in small characters below or adjacent to the other marking specified. If there is limited space, the marking may be shortened to "U.S.A.".

**3.7.6 Date code.** Microcircuits shall be marked with a unique code to identify the first or the last week of the period during which devices in that inspection lot were sealed. The first two numbers in the code shall be the last two digits of the number of the year, and the third and fourth numbers shall be two digits indicating the calendar week of the year.

**3.7.7 Marking location and sequence.** The QML mark, the part number, and ESDS identifier shall be located on the top surface of leadless or leaded chip carriers, pin grid array packages, flat packages or dual-in-line configurations and on either the top or the side of cylindrical packages (TO configurations and similar configurations). When the size of a package is insufficient to allow marking of special process identifiers on the top surface, the backside of the package may be used for these markings except the ESDS identifier shall be marked on the top. Button cap flat packs with less than or equal to 16 leads may have the identifier marked on the ceramic. Backside marking with conductive or resistive ink shall be prohibited.

**3.7.7.1 Beryllium oxide package identifier.** If a microcircuit package contains beryllium oxide, the part shall be marked with the designation "BeO".

**3.7.7.2 Electrostatic discharge sensitivity identifier.** A device's ESDS class determined by the electrostatic discharge sensitivity classification test, test method 3015 of MIL-STD-883, shall be marked as follows:

- a. Class 1 - 1999 V and below - single equilateral triangle outline (still acceptable as pin one designator).
- b. Class 2 - 2000 V - 3999 V - double equilateral triangle outline (still acceptable as pin one designator).
- c. Class 3 - 4000 V and above - no designator.

**3.7.8 Marking on container.** All of the markings specified in 3.7 through 3.7.6, except the index point, shall appear on the carrier, unit pack (e.g., individual foil bag), unit container, or multiple carriers (e.g., tubes, rails, magazines) for delivery and this marking shall be in accordance with MIL-STD-129 and MIL-M-55565 for ESDS microcircuits. In addition, the EIA-STD-RS-471 symbol for ESDS devices may also be marked on the carrier or container. However, if all the marking specified above is clearly visible on the devices and legible through the unit carrier or multiple carrier, or both then the ESD marking only (in accordance with MIL-STD-1285) shall be required on the multiple carrier. These requirements apply to the original or

repackaged QML microcircuit by the manufacturer or distributor. In addition, for lots held by manufacturers and their authorized distributors' for more than 36 months following the date code (see 3.7.9), a similar code identifying subsequent reinspection dates shall be applied to the lowest level of packaging which contains a single inspection lot date code of unit carriers, unit packs, unit containers or multiple carriers.

**3.7.9 Marking option for controlled storage.** Where microcircuits are subjected to testing and screening in accordance with some portion of the quality assurance requirements and stored in controlled storage areas pending receipt of orders requiring conformance to the QM plan, the date code shall be placed on the microcircuit package along with the other markings specified in 3.7 sufficient to assure identification of the material. As an alternative, if the microcircuits are stored together with sufficient data to assure traceability to processing and inspection records, all markings may be applied after completion of all inspections.

**3.8 Remarking.** QML microcircuits shall be remarked when required and approved by the TRB. All remarking procedures shall be in accordance with 3.7 herein.

**3.9 Workmanship.** Microcircuits shall be manufactured, processed, and tested in a careful and skillful manner in accordance with good engineering practice, with the requirements of this specification, and with the production practices, workmanship instructions, inspection and test procedures, and training aids prepared by the manufacturer in fulfillment of the quality assurance program.

#### **4. QUALITY ASSURANCE PROVISIONS**

**4.1 Responsibility for inspection.** Unless otherwise specified in the contract or purchase order, the contractor is responsible for the performance of all inspection requirements (examinations and tests) as specified herein. Except as otherwise specified in the contract or purchase order, the contractor may use his own or any other facilities suitable for the performance of the inspection requirements specified herein, unless disapproved by the Government. The Government reserves the right to perform any of the inspections set forth in this specification where such inspections are deemed necessary to ensure supplies and services conform to prescribed requirements.

**4.2 Quality and reliability assurance.** This section details the manufacturing requirements that each individual QML integrated circuit designed, manufactured and tested on a certified QML technology flow must meet in order to be identified as QML. Also defined are the screens to which each QML integrated circuit must be subjected to and pass (see 4.3). In order to show that the technology continually meets the certified quality, reliability and performance capabilities, technology conformance inspection (TCI) requirements (see 4.4) are outlined.

**4.2.1 Manufacturing processes.** Manufacturing processes involve all certified processes (i.e., design, fabrication, package, etc.) necessary to manufacture quality and reliable QML integrated circuits to the performance requirements of the device procurement specification (see 3.6). The manufacturer must assure that only certified processes and qualified technologies are used for QML integrated circuits. Listed in the following paragraphs are specific requirements which must be documented by the manufacturer to have been completed on each QML integrated circuit designed, manufactured and tested on a QML line.

**4.2.2 Traceability.** Traceability to the wafer lot level shall be provided for all delivered microcircuits. Traceability shall document, as a minimum, the completion of each step required in design, fabrication, assembly, test and any applicable qualified rework procedure.

4.2.3 Incoming inspection. Incoming inspection and test procedures shall be in place to insure conformance of the material to the material specifications. Inspection reports and test data shall be maintained on file for review by the qualifying activity. Failure reports shall be generated for material failing incoming inspection and test. A corrective action plan shall be in place to identify the causes of failure and effect changes to improve future material. If the manufacturer has extended the QM program to suppliers, then the supplier failure analysis and corrective action plan, after TRB approval, are recognized.

4.2.4 ESDS control. QML microcircuits shall be handled in accordance with MIL-HDBK-263 and MIL-STD-1686 to safeguard against discharge damage.

4.2.5 Design requirements. The manufacturer shall show evidence that, as a minimum, the following controlled processes and checkpoints are being accomplished each time a microcircuit is processed through the design system. The design system must be certified to 3.5 requirements and must be under configuration control. The specific requirements are shown below:

<u>Design</u>	<u>Requirements (paragraph)</u>
Device procurement specification <sup>1/</sup>	3.6
Simulation - model verification	3.5.1.3.1a
Layout verification	3.5.1.3.1b
Stability and fault coverage verification	3.5.1.3.1d and test method 5012 of MIL-STD-883
Electrical parameter performance extraction	3.5.1.3.1c
Archived data	3.5.1.4.3f

#### 4.2.6 Fabrication requirements

4.2.6.1 Mask requirements (when applicable). All procedures used to manufacture masks for monolithic fabrication shall be certified. If mask shop is internal to the manufacturing organization, all designs shall be checked for errors utilizing appropriate design rule checkers before start of the mask making. In all cases, the completed mask shall be inspected for flaws and errors upon receipt from the mask shop. The final photolithographic mask to be used for QML microcircuit wafer fabrication shall be compliant with the critical dimensions. Measurements shall show that the pattern sizes and positions are consistent with the design rules. All masks shall be maintained under an inventory control program which outlines the inspection and the release of masks to fabrication, recording of usage, cleaning cycles, and maintenance repair. All conditions for removal of masks from inventory shall be documented.

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<sup>1/</sup> For RHA devices, sample testing of each design to verify PIPL shall be accomplished to determine dose rate upset threshold, latchup immunity (when specified) at maximum temperature and voltage, and linear energy threshold (LET) for upset and latchup as well as the cross section for SEP. If simulation models can be verified to address these concerns, they would be acceptable.



**4.2.6.2 Wafer fabrication process.** All microcircuits manufactured on a QML line shall be processed on a certified fabrication line. The wafer fabrication process shall be monitored and controlled using a standard evaluation circuit (SEC), technology characterization vehicle (TCV) and parametric monitors (PM) in accordance with 3.5 herein. The wafer fabrication sequence to produce finished wafers shall be established with processing limits for each wafer fabrication step. These limits shall be certified. Specific requirements are detailed below:

<u>Procedure</u>	<u>Requirements (paragraph)</u>
Traceability	3.5.1.4.2k, 4.2.2
Lot travelers	As required (TRB determined)
Glassivation	3.5.1.3.2
Parametric monitors	3.5.1.3.2e
Wafer acceptance	3.5.1.3.3
Standard evaluation circuits	3.5.1.3.2d
Technology characterization vehicles	3.5.1.3.2b
Rework	Photoresistive only
Internal conductors and metallization thickness	Current density requirements

**4.2.7 Assembly and package requirements.** All devices shall be assembled in a facility which has been certified. As a minimum, all material, package (see 3.5.1.3.6) assembly processes and environmental controls must be documented and in place to meet the quality and reliability requirements of QML microcircuits.

**4.2.7.1 Package design selection reviews.** The manufacturer shall establish and implement systematic package design or selection reviews to ascertain compatibility of chip(s) and packages with respect to thermal, electrical and mechanical performance and manufacturing, testing, and reliability requirements. These reviews shall also insure the product realization process (PRP) meets the acquiring activity requirements and shall be documented.

**4.2.7.1.1 Package requirements.** All QML microcircuits shall be assembled in packages which belong to a certified package technology style as classified by the TRB.

4.2.7.2 Assembly process procedures. The following assembly process procedures, shall be used, as applicable, to assemble QML microcircuits. The manufacturer shall control all phases of the assembly line to ensure that contamination from any source or equipment operation and human intervention does not degrade the reliability of the assembly process or QML microcircuit. Specific requirements are shown below:

<u>Assembly and package procedure</u>	<u>Requirements</u>
Incoming inspection	3.5.1.3.5a
Eutectic die attach	Test method 2010, 3.5.1.3.5a
Non-eutectic die attach	Test method 2010, 3.5.1.3.5a, Test method 5011 (as applicable)
Internal visual	Test method 2010, 3.5.1.3.5a
Hermeticity	Test method 1014, test method 1018
Handling	3.5.1.3.5a
Human contamination	3.5.1.3.5a
Rework	3.5.1.3.5a, 4.2.7.3
Internal water vapor content	Test method 1018, 3.5.1.3.5c

4.2.7.3 Assembly rework requirements. All QML microcircuits rework procedures shall be certified. Only rebonding of wires bonded with manual wire bonding equipment is permitted on microcircuit assemblies prior to lid seal. No delidding or package opening for rework shall be permitted for QML microcircuits. Allowable rework of sealed packages includes recleaning of any microcircuit or portion thereof, any remarking to correct defective marking and lead straightening.

4.2.8 Electrical test. All QML microcircuits shall be electrically tested over the specified temperature range in accordance with the device procurement specification in a certified test facility before delivery of the product.

4.3 Screening. All QML integrated circuits shall be subjected to and pass the screens specified in table IX, herein. The procedures and accept and/or reject criteria for the table IX screens shall have been certified by the qualifying activity. The manufacturer, through its TRB, may elect to eliminate or modify a screen based on empirical reliability data which indicates that for the QML technology, the change is justified. If such a change is implemented, the manufacturer is still responsible for providing product which meets all of the performance, quality, and reliability requirements herein. Notification of such changes, deviations or eliminations must be made to the qualifying activity in accordance with 3.4.3.2 requirements.

4.3.1 Screen testing failures. Devices which fail any screen test shall be removed at the time of observation or immediately at the conclusion of the test in which the failure was observed. Once rejected and verified as a device failure, no retesting is allowed. Use of electrical rejects for nonelectrical tests must meet the certified procedures and shall be the exception. Catastrophic failures (i.e., shorts or opens measurable or detectable at 25°C) subsequent to burn-in shall be analyzed. Analysis of catastrophic failures may be limited to a quantity and degree sufficient to establish failure mode and cause and the results shall be documented and made available to the qualifying activity. A summary of the results shall be included in the status report.

4.3.2 Screening resubmission criteria. When it has been established that a failures during screening tests is due to operator error or equipment failure and it has been established that the remaining QML microcircuits have not been damaged or degraded, the surviving microcircuits, as the case may be, may be resubmitted to the corrected screening test(s) in which the error occurred. Failures verified as having been caused by test equipment failure or operator error shall not be counted in the PDA calculation (when applicable). ESD failures shall be counted as rejects and shall not be attributed to equipment failure or operator error.

**4.3.3 Electrostatic discharge sensitivity.** Electrostatic discharge sensitivity testing shall be done in accordance with test method 3015 of MIL-STD-883, and the device specification, and marked in accordance with the marking provisions in 3.7 herein. Unless otherwise specified, tests shall be performed for initial qualification and product redesign as a minimum. Devices shall be handled in accordance with MIL-HDBK-263 and MIL-STD-1686 to safeguard against discharge damage (see 3.5.1.3.4).

**4.3.4 Internal visual inspection.** Internal visual inspection shall be performed to the requirements of test method 2010, condition B of MIL-STD-883. Microcircuits awaiting preseat inspection, or other accepted, unsealed microcircuits awaiting further processing shall be stored in a dry, inert, controlled environment until sealed. The alternate procedure of test method 5004 of MIL-STD-883 shall be used when any of the following criteria are met:

- a. Minimum horizontal geometry is less than three microns.
- b. Metallization consists of two or more levels.
- c. Opaque materials mask design features.

**4.3.5 Constant acceleration.** All microcircuits shall be subjected to constant acceleration, in the Y1 axis only, in accordance with test method 2001, condition E (minimum) of MIL-STD-883. Microcircuits which are contained in packages which have an inner seal or cavity perimeter of two inches or more in total length or have a package mass of five grams or more may be tested by replacing condition E with condition D in method 2001.

**4.3.6 Burn-in.** Burn-in shall be performed on all QML microcircuits at their maximum rated operating temperature. For microcircuits whose maximum operating temperature is stated in terms of ambient temperature,  $T_A$ , table I of test method 1015 of MIL-STD-883 applies. For microcircuits whose maximum operating temperature is stated in terms of case temperature,  $T_C$ , and where the ambient temperature would cause  $T_J$  to exceed  $+175^\circ\text{C}$ , the ambient operating temperature may be reduced during burn-in from  $+125^\circ\text{C}$  to a value that will demonstrate a  $T_J$  between  $+175^\circ\text{C}$  and  $+200^\circ\text{C}$  and  $T_C$  equal to or greater than  $+125^\circ\text{C}$  without changing the test duration. Data supporting this reduction shall be available to the acquiring and qualifying activities upon request.

**4.3.7 Final electrical measurements.** Final electrical testing of microcircuits shall assure that the microcircuits tested meet the electrical requirements of the device procurement specification and shall include, as a minimum, the tests of Group A, subgroups 1, 2, 3, 4 or 7, 5 and 6 or 8, and 9, 10 and 11.

**4.3.8 Seal (fine and gross leak) testing.** Fine and gross leak seal tests shall be performed between temperature cycling and final electrical testing after all shearing and forming operations on the terminals in accordance with MIL-STD-883 method 1014.

**4.3.9 Pattern failures.** Pattern failure criteria may be used as an option for any screen provided that:

- a. Inspection lot size is less than 500 microcircuits.
- b. Preburn-in testing is done.

A maximum number of pattern failures (failures of the same part type when the failures are caused by the same basic failure mechanism) shall apply as specified in the acquisition document. If not otherwise specified, the maximum allowable pattern failures shall be five. Accountability shall include burn-in through final electrical test.

4.3.9.1 Pattern failure rejects. When the number of pattern failures exceeds the specified limits, the burn-in lot shall be rejected. At the manufacturer's TRB option, the rejected lot may be resubmitted to burn-in one time provided:

- a. The cause of the failure has been determined and evaluated.
- b. Appropriate and effective corrective action has been completed to reject all microcircuits affected by the failure cause.
- c. Appropriate preventive action has been initiated.

4.4 Technology conformance inspection (TCI). TCI testing shall be accomplished by the manufacturer on a periodic basis to assure that the manufacturer's quality, reliability, and performance capabilities meet the requirements of the QM plan. The manufacturer of QML microcircuits shall be certified by the qualifying activity to use one or both of the technology conformance inspection (TCI) procedures described below. The two TCI procedures are end-of-line QCI (option 1) and in-line control (option 2).

4.4.1 General. Any QML or SEC integrated circuit used for either TCI option (see 4.4.2 or 4.4.3) must be screened in accordance with 4.3 requirements.

4.4.1.1 TCI reporting. Summary of TCI tests analysis shall be submitted to the qualifying activity in accordance with 3.4.5 requirements. If TCI requirements are not met, the technology review board shall notify the qualifying activity immediately and all products manufactured and delivered between the last TCI and the failed TCI shall be placed in suspect status. The manufacturer shall analyze the failure, determine the reason for failure and submit a corrective action plan. An assessment of whether to recall all suspect products shall be made by the TRB and the qualifying activity shall be notified of the decision. Recertification and requalification of the QML line may be required based on the nature of the problem and action taken by the manufacturer. Procedures for standard QCI and in-line control for a QML line are described in the following paragraphs.

4.4.2 Standard quality conformance inspection testing (option 1). End-of-line QCI testing shall be performed every QCI interval, as recommended in table VIII herein. Each end-of-line QCI vehicle shall pass the end-of-line quality conformance. All group A, B and E testing shall be performed on microcircuits to be delivered as QML microcircuits. Group C and D testing shall be done on either the SEC or QML microcircuits. Groups A, B, C, D, and E requirements are found in tables III thru VII, herein.

NOTE: If a manufacturer elects to eliminate a quality conformance inspection step by substituting an in-process control or statistical process control procedure, the manufacturer is only relieved of the responsibility of performing the QCI operation associated with that step. The manufacturer is still responsible for providing a product which meets all of the performance, quality, and reliability requirements herein and in the device procurement specification. Documentation supporting substitution for QCI shall be retained by the manufacturer and available to the qualifying activity upon request.

Each group may contain individual subgroups for the purposes of identifying individual tests or groups of tests. Subgroups within a group of tests may be performed in any sequence but individual tests within a subgroup (except group B, subgroup 2) shall be performed in the sequence indicated for groups B, C, D, and E tests herein. Electrical reject devices from the same inspection lot may be used for all subgroups when electrical end-point measurements are not required.

4.4.2.1 Group A inspection. Group A inspection shall be performed on each inspection lot and shall consist of electrical parameter tests specified for the specified device. Group A inspection may be performed in any order.

4.4.2.2 Group B inspection. Group B inspection shall be performed on each inspection lot, for each qualified package type and lead finish. Group B shall consist of mechanical and environmental tests for the specified device class. Resubmission procedures shall be documented in the QM plan. For solderability, a statistical sound sample size consisting of leads from several packages shall be tested with zero (0) failures. The actual number shall be determined by the TRB and detailed in the TCI procedures in the QM plan.

4.4.2.3 Group C inspection. Group C inspection shall include die-related tests specified which are performed periodically. Resubmission procedures shall be documented in the QM plan. Where group C endpoints are done on actual devices, group C endpoints shall be specified in the device procurement specification.

4.4.2.4 Group D inspection. Group D inspection shall include package related tests which are performed periodically. Resubmission procedures shall be documented in the QM plan. Where group D endpoints are done on actual devices, group D endpoints shall be specified in the device procurement specification.

4.4.2.5 End-point tests for groups B, C, D, (E if applicable). End-point measurements and other specified post-test measurements shall be made for each sample after completion of all other specified tests in the subgroup. The test limits for the end-point measurements shall be the same as the test limits for the respective group A subgroup inspections. Different end-points may be specified for group E tests in the detail specifications. Any additional end-point electrical measurements may be performed at the discretion of the manufacturer.

4.4.2.6 End-of-line QCI testing. All microcircuits used in end-of-line QCI testing that meet the requirements of this document and the device procurement specification shall be identified and delivered to the acquiring activity as QML microcircuits upon approval of the manufacturer's TRB.

4.4.3 In-line control testing (option 2). In-line control testing shall be performed through the use of the approved SEC or QML microcircuit. The in-line control test plan shall show how all the group A, B, C and D, test conditions are incorporated under SPC or process control to allow in-line control monitoring. Group E tests shall be done on each QML microcircuits as applicable. The following shall also apply.

4.4.3.1 Group A electrical testing. Group A electrical testing shall be satisfied by in-line inspections performed in accordance with the applicable procedure of MIL-STD-883 on actual devices.

4.4.3.2 Group C life tests. Life tests shall be performed on the SEC at intervals set by the TRB in the quality management plan.

TABLE III. Group A electrical tests. 1/

Subgroup	Parameters	Quantity (accept no.)
1	Static test at +25°C	116(0)
2	Static tests at maximum rated operating temperature	116(0)
3	Static tests at minimum rated operating temperature	116(0)
4	Dynamic test at +25°C	116(0)
5	Dynamic tests at maximum rated operating temperature	116(0)
6	Dynamic tests at minimum rated operating temperature	116(0)
7	Functional test at +25°C	116(0)
8	Functional tests at maximum and minimum rated operating temperatures	116(0)
9	Switching tests at +25°C	116(0)
10	Switching tests at maximum rated operating temperature	116(0)
11	Switching tests at minimum rated operating temperature	116(0)

1/ The specific parameters to be included for tests in each subgroup shall be as specified in the device procurement specification. Where no parameters have been identified in a particular subgroup or test within a subgroup, no group A testing is required for that subgroup or test to satisfy group A requirements.

TABLE IV. Group B tests.

Subgroup	MIL-STD-883			Minimum sample size Quantity (accept no.)
	Test	Method	Condition	
1	Resistance to solvents	2015	A or B	4(0)
2	Bond strength (1) Thermo compression (2) Ultrasonic (3) Flip-chip (4) Beam lead Die shear test	2011     2019	 (1) C or D (2) C or D (3) F (4) H die size	22(0)
3	Solderability	2003 or 2022	solder temperature 245°C ±5°C	See 4.4.2.2

TABLE V. Group C tests.

Test	MIL-STD-883		Quantity (accept no.)
	Method	Condition	
Subgroup 1 a. Steady state life test  b. End-point electrical parameters	1005	Test condition to be specified (1,000 hrs at 125°C)  As specified in the applicable device procurement specification	45(0)

TABLE VI. Group D tests.

Subgroup	Test	MIL-STD-883		Quantity (accept no.)
		Method	Condition	
1	a. Physical dimensions	2016		15(0)
2	a. Lead integrity	2004	B2 Fatigue	15(0)
	b. Seal			
	(1) Fine	1014	As applicable	
	(2) Gross	1014	As applicable	
3	a. Thermal shock	1011	B, 15 cycles	15(0)
	b. Temperature cycling	1010	C, 100 cycles	
	c. Moisture resistance	1004		
	d. Seal	1014	As applicable	
	(1) Fine			
	(2) Gross			
	e. Visual	1004, 1010	As specified in the applicable device procurement specification	
	f. End-point electricals			
4	a. Shock	2002	B	15(0)
	b. Vibration, variable frequency	2007	A	
	c. Acceleration	2001	E, Y1 orientation	
	d. Seal	1014	As applicable	
	(1) Fine			
	(2) Gross			
	e. Visual examination		As specified in the applicable device procurement specification	
	f. End-point electricals			
5	a. Salt atmosphere	1009	A	15(0)
	b. Seal	1014	As applicable	
	(1) Fine			
	(2) Gross			
	c. Visual	1009	(Visual criteria)	
6	a. Internal water vapor	1018	5000 ppm 100°C	3(0) or 5(1)
7	a. Adhesion of lead finish	2025		15(0)
8	a. Lid torque	2024	glass frit seal only	5(0)

TABLE VII. Center group E (RHA testing)(radiation hardness assurance tests) 1/

Test	MIL-STD-883		RHACL/SPEC 4/	Quantity 3/ (accept no.)
	Method	Condition		
Subgroup 1 Neutron 2/ irradiation  Endpoint electrical parameters	1017	+25°C  As specified in the applicable device procurement specification	>10 >2 ≤10	0(0) 5(0)
Subgroup 2 Total ionizing radiation dose  Endpoint electrical parameters	1019	+25°C  As specified in the applicable device procurement specification	>10 >2 ≤10	0(0) 5(0)

1/ Parts used for one subgroup test may not be used for other subgroups but may be used for higher levels in the same subgroup. Total dose exposure shall not be considered cumulative unless testing is performed within the time limits of the test method.

2/ Not required for MOS devices unless bipolar elements are included by design.

3/ Per wafer lot. Alternatively, each wafer may be accepted on a 2(0) quantity (accept) number. If the alternate is chosen, a PDA of 10% or equivalent shall apply to the lot.

4/ The RHACL/SPEC is the ratio of the capability level to the specification level of fluence.

TABLE VIII. Standard QCI testing procedure. 1/

Table	QCI requirements	QCI vehicle	Interval
Table III	Group A electrical testing	Actual device	Each inspection lot
Table IV	Group B testing	Actual device	Each inspection lot
Table V	Group C testing	SEC or actual device	Every 3 months
Table VI	Group D testing	SEC or actual device	Every 6 months
Table VII	Group E testing	Actual device	Each wafer lot

1/ Each group may contain individual subgroups for the purposes of identifying individual tests or groups of tests.



TABLE IX. Microcircuit screening procedure for QML microcircuits.

Screen	MIL-STD-883 test method and condition
Electrostatic discharge sensitivity	3015 (see 4.3.3, initial qualification only)
Wafer acceptance	TRB plan (see 3.5.1.3.3)
Internal visual	2010, test condition B (see 4.3.4)
Temperature cycling	1010, test condition C, 50 cycles minimum
Constant acceleration	2001, test condition E (minimum) Y1 orientation only (see 4.3.5)
Serialization	In accordance with device procurement specification
Burn-in test	1015, 160 hrs at +125°C minimum (see 4.3.6)
Interim (pre-burn-in) electrical parameters	In accordance with device procurement specification
Interim (post-burn-in) electrical parameters	In accordance with device procurement specification
Percent defective allowable (PDA) calculation	5% or TRB determined, all lots (subgroup 1 table III)
Final electrical test	In accordance with device procurement specification
a. Static tests (table III)	
1. +25°C	
2. Maximum and minimum rated operating temperature	
b. Dynamic or functional tests (table III)	
1. +25°C	
2. Maximum and minimum rated operating temperature	
c. Switching tests (table III)	
1. +25°C	
2. Maximum and minimum rated operating temperature	
Seal	1014
a. Fine	
b. Gross	
External visual	2009

5. PACKAGING.

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-55565.

## 6. NOTES

6.1 Intended use. This specification is intended to support government microcircuit application and logistic programs. Detailed characteristics of microcircuits needed for a program are to be defined by the device procurement specification.

6.2 Terms and definitions. For the purpose of this specification, the terms, and definitions of MIL-STD-883 and MIL-STD-1331, and those contained herein shall apply and shall be used in the applicable device procurement specifications wherever they are pertinent.

6.2.1 Microelectronics. That area of electronic technology associated with or applied to the realization of electronic systems from extremely small electronic parts or elements.

6.2.2 Element (of a microcircuit or integrated circuit). A constituent of the microcircuit or integrated circuit that contributes directly to its operation.

6.2.3 Substrate (of a microcircuit or integrated circuit). The supporting material upon or within which the elements of a microcircuit or integrated circuit are fabricated or attached.

6.2.4 Integrated circuit (microcircuit). A small circuit having a high equivalent circuit element density, which is considered as a single part composed of interconnected elements on or within a single substrate to perform an electronic circuit function.

6.2.4.1 Multichip microcircuit. An integrated circuit or microcircuit consisting of elements formed on or within two or more semiconductor chips which are separately attached to a substrate or package.

6.2.4.2 Monolithic microcircuit. An integrated circuit or microcircuit consisting exclusively of elements formed in situ on or within a single semiconductor substrate with at least one of the elements formed within the substrate.

6.2.5 Microcircuit module. An assembly of integrated circuits or an assembly of integrated circuits and discrete parts, designed to perform one or more electronic circuit functions, and constructed such that for the purposes of specification testing, commerce, and maintenance, it is considered indivisible.

6.2.6 Production lot. A production lot shall consist of devices manufactured on the same production line(s) (QM technology flow) by means of the same production technique, materials, controls, and design.

6.2.7 Inspection lot. A quantity of integrated circuits submitted at one time for inspection to determine compliance with the requirements and acceptance criteria of the applicable device procurement specification. Each inspection lot shall be manufactured on the same production line through final seal by the same production techniques.

6.2.8 Wafer lot. A wafer lot consists of integrated circuit wafers formed into a lot at the start of wafer fabrication for homogeneous processing as a group, and assigned a unique identifier or code to provide traceability.

6.2.9 Percent defective allowable (PDA). Percent defective allowable is the maximum observed percent defective which will permit the lot to be accepted after the specified 100 percent test.

6.2.10 Delta limit. The maximum change in a specified parameter reading which will permit a device to be accepted on the specified test, based on a comparison of the present measurement with a specified previous measurement. Note: When expressed as a percentage value, it shall be calculated as a proportion of the previous measured value.

6.2.11 Rework. Any processing or reprocessing operation documented in accordance with the manufacturer's QM plan, other than testing, applied to an individual device, or part thereof, and performed subsequent to the prescribed nonrepairing manufacturing operations which are applicable to all devices of that type at that stage.

6.2.12 Final seal. That manufacturing operation which completes the enclosure of a device so that further internal processing cannot be performed without disassembling the device.

6.2.13 Acquiring activity. The organizational element which contracts for articles, supplies, or services; or it may be a contractor or sub-contractor when the organizational element has given specific written authorization to such contractor or subcontractor to serve as agent of the acquiring activity. A contractor or subcontractor serving as agent of the acquiring activity shall not have the authority to grant waivers, deviations, or exceptions to this specification unless specific written authorization to do so has been given by the organization (i.e., preparing activity, qualifying activity).

6.2.14 Qualifying activity. The organizational element of the Government that grants certification, and qualification for the specific technology flow in accordance with this specification.

6.2.15 Parts per million (PPM). Parts per million shall be as defined in JEDEC Publication 16.

6.2.16 Device type. The term device type refers to a single specific microcircuit configuration.

6.2.17 Die type. A microcircuit manufactured using the same physical size, materials, topology, mask set, process flow, on a single fabrication line.

6.2.18 Radiation hardness assurance (RHA). The portion of product assurance which insures that parts continue to perform as specified or degrade in a specified manner when subjected to the specified radiation environmental stress.

6.2.19 Electrostatic discharge sensitivity (ESD). Electrostatic discharge sensitivity is defined as the level of susceptibility of a device to damage by static electricity. The level of susceptibility of a device is found by ESDS classification testing and is used as the basis for assigning on ESDS class.

6.2.20 Package family. A group of package types with identical configuration and process techniques (e.g. cerdip, side braze, cerpack).

6.2.21 Technology flow. A technology flow is that specific manufacturing line from design, fabrication, assembly, packaging, and test in a given technology from which a manufacturer designs, builds, and tests integrated circuits. Once a manufacturer's technology flow has been certified and qualified by the qualifying activity, it is listed on the Qualified Manufacturer's Listing (QML).

6.2.22 Qualified manufacturer's listing (QML). The qualified manufacturer's listing is that listing which defines and specifies the certified and qualified technology flow of a manufacturer from which QML integrated circuits may be purchased.

6.3 Discussion. The foundation of generic qualification is the instillment of quality management (QM) within the manufacturing environment. Quality management (QM) requires that all levels of management and nonmanagement be actively involved in the commitment to quality. Also, a technology review board (TRB) must be established to control, stabilize, monitor and improve the qualified technology. The TRB shall develop a quality management plan that outlines how the manufacturing operation for a given technology is controlled, monitored and improved throughout its entire "life cycle". Key aspects of this plan are the establishment of statistical process control, field failure return programs, corrective action procedures, quality improvement and any other approaches required to control and improve product quality and reliability. These requirements are detailed in this document.

Further, this document describes procedures and requirements for manufacturer's listing on the Qualified Manufacturer List (QML) for integrated circuits. Manufacturers listed on the QML will be able to produce microcircuits without the need for extensive end-of-manufacturing qualification testing and quality conformance inspections on each device design. The reduction of the end-of-manufacturing testing will be replaced with in-line monitoring and testing and statistical process controls (SPC). Also, surrogate devices, such as the standard evaluation circuit (SEC) will be used to assess the technology's reliability. Introduction of this methodology shifts the emphasis from the need of individual microcircuit qualification to process (technology) certification and qualification. This will accelerate the microcircuit insertion cycle of high quality and reliable microcircuits.

The generic qualification philosophy, leading to QML, is a process by which a manufacturer acquires a manufacturing line or technology flow certification and qualification. Ongoing monitoring techniques will be used to maintain QML status. The manufacturing line consists of facilities and procedures appropriate to accomplish the design, mask making, wafer fabrication, assembly, package and testing of microcircuits (see figure 2). Figure 3 illustrates six possible combinations of a manufacturing line utilizing three design centers, two mask fabrication facilities, three wafer fabrication facilities, two package and assembly sites and two test facilities. The procedure of generic qualification is accomplished in two stages; certification and qualification. The process of certification is the recognition of evidence by the qualifying activity that the manufacturing line is capable of producing microcircuits of high quality and compliant with the requirements of this document. Qualification is the actual demonstration of the certified manufacturing line capabilities by producing "first pass" microcircuits compliant with the requirements of this document and the device specification. In figure 3, each block can be individually reviewed, but must be certified as a flow. The only process flow which would be qualified (QML listed) would be the group of blocks which are linked together and tested during qualification. The letters "A" and "B" indicate a QML flow where qualification testing has qualified a complete path. The other paths are not QML until certification and qualification testing of the processes is done.

QM does not stop with a manufacturer listed on the QML. This specification identifies the necessary screens which still must be done on each device built. These screens can be reduced or changed by the manufacturers' TRB when gathered reliability data on the technology indicates that such changes are substantiated. The philosophy of generic qualification incorporates the idea that high quality and reliable microcircuits can be obtained without excessive testing if the processes are properly monitored and controlled at each step of the manufacturing line. The following describes the monitors and controls which may be used.

- a. The design procedure and tools are controlled in such a manner that the ensuing microcircuit design performs only with limits that have been shown to be reliable for the technology being used, within the constraints of established design rules (electrical, geometric and reliability).
- b. The mask fabrication facility is controlled such that an error free mask is produced from the microcircuit design database. Monitoring, controlling and reducing defect density is helpful in obtaining error free masks.
- c. The wafer fabrication process is controlled with the following: use of in-line statistical control; a parametric monitor (PM) structure for measuring electrical parameters; a technology characterization vehicle (TCV) structure to study intrinsic reliability mechanisms; and a standard evaluation circuit (SEC) to monitor the fabrication process and to serve as a surrogate microcircuit for reliability testing.
- d. The package and assembly facility is controlled with emphasis on in-line statistical process control of all assembly steps.
- e. The test area controls consist of test equipment accuracy and calibration as well as a controlled interface to the microcircuit design center.

- f. The overall control of the processes are under the auspices of a technology review board (TRB) which is established by the manufacturer. The TRB is solely responsible for the QML flow that has been certified and qualified.
- g. For radiation hardness assurance (RHA) devices, procedures and requirements are integrated into this document for establishing and demonstrating a radiation hardness assurance capability level (RHACL) for the technology. Many device oriented tests can be reduced or eliminated when correlation data for models and test structures have been established by the TRB. The main concern in the RHA community is whether the device specification accurately describes the device performance in the radiation environment specified. Until such models and test structures are developed, some actual device radiation testing will be required.
- h. Appendix B to this specification defines an implementation transition approach which may be used for space or other critical environment applications.

6.4 Additional reference documents. The following documents are not directly referenced herein but should be used as guidelines.

- DHA-TR-36-38 - Hardness Assurance Guidelines for MIL-HDBK-339 (USAF).
- FED-STD-209 - Clean Room and Work Station Requirements, Controlled Environments.
- MIL-HDBK-279 - Total Dose Hardness Assurance Guidelines for Semiconductors and Microcircuits.
- MIL-HDBK-280 - Neutron Hardness Assurance Guidelines for Semiconductors and Microcircuits.
- MIL-HDBK-339 - Custom Large Scale Integrated Circuit for Space Applications.
- MIL-STD-45662 - Calibration Systems Requirements.
- AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)
- ASTM B487-79 - Measurement of Metal and Oxide Coating Thicknesses by Microscopical Examination of a Cross Section.
- ASTM B567-79A - Measurement of Coating Thickness by the Beta Backscatter Method.
- (Application for copies should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)
- ELECTRONIC INDUSTRIES ASSOCIATION (EIA)
- EIA-STD-5 - Packaging Materials Standard for Protection of Electrostatic Discharge Sensitive Devices.
- JEDEC Publication
- 95 - JEDEC Registered and Standard Outlines for Semiconductor Devices.
- 16 - Assessment of Microcircuit Outgoing Quality Levels in Parts Per Million (PPM).

(Application for copies should be addressed to the Electronic Industries association, 2001 Eye Street, N.W., Washington, DC 20006.)



FIGURE 2. The OML manufacturing line.

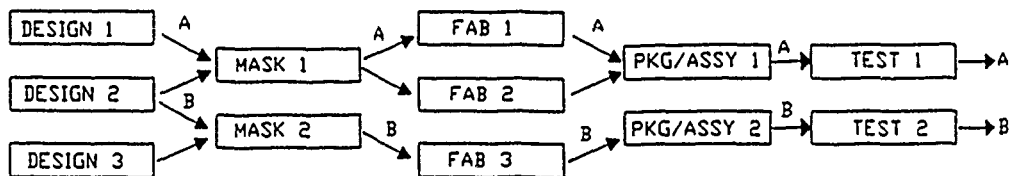


FIGURE 3. Combinations of a manufacturing line.

6.5 Subject term (key word) listings:

Application specific integrated circuit (ASIC)  
Computer automated design (CAD)  
Design-for-test (DFT)  
Design rule check (DRC)  
Electrical rule check (ERC)  
Electrostatic discharge sensitivity (ESD)  
Failure analysis (FA)  
Joint test action group (JTAG)  
Linear energy threshold (LET)  
Mean-time-to-failure (MTF)  
Original equipment manufacturer (OEM)  
Parametric monitor (PM)  
Post irradiated endpoint parameter limits (PIPL)  
Qualified manufacturer listing (QML)  
Quality assurance (QA)  
Quality management (QM)  
Radiation hardness assurance (RHA)  
Radiation hardness assurance capability level (RHACL)  
Single event phenomena (SEP)  
Single event upset (SEU)  
Standard evaluation circuit (SEC)  
Statistical process control (SPC)  
Technology characterization vehicle (TCV)  
Technology conformance inspection (TCI)  
Technology review board (TRB)  
Tester independent support software system (TISSS)  
Time dependent dielectric breakdown (TDDB)  
Very high speed integrated circuit (VHSIC)  
VHSIC hardware description language (VHDL)

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## APPENDIX A

### DEVICE PROCUREMENT SPECIFICATION

#### 10. SCOPE

10.1 Scope. This appendix contains the details of the device procurement specification requirements needed to define individual microcircuit types for procurement. This appendix is a mandatory part of the specification.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

#### 30. DEVICE PROCUREMENT SPECIFICATION

30.1 Scope. This drawing describes device requirements in accordance with MIL-I-38535 QML devices.

30.2 PIN. The complete part or identifying number (PIN) shall be in accordance with MIL-I-38535 (see 3.7.2.).

30.2.1 Device types. The device types shall identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
--------------------	-----------------------	-------------------------

30.2.2 Case outlines. The case outlines shall be designated as appropriate to the requirements of MIL-I-38535 and as follows:

<u>Outline letter</u>	<u>Case outline</u>
-----------------------	---------------------

30.2.3 Lead finish. The lead finish shall be as specified in MIL-I-38535.

30.3 Absolute maximum ratings for usage. 1/

- Operating temperature range
- Positive supply voltage
- Negative supply voltage
- Input voltage
- Power dissipation ( $P_D$ )
- Storage temperature range
- Lead temperature (soldering, 10 seconds)
- Thermal resistance, junction-to-case ( $\theta_{JC}$ )
- Electrostatic discharge sensitivity (ESDS)
- G-Force
- Other parameters (device specific)

30.4 Recommended operating conditions.

- Operating temperature range (case ( $T_C$ ) or ambient ( $T_A$ ) as appropriate for technology)
- Supply voltages
- Other parameters (device specific)

---

1/ Stresses above the absolute maximum ratings may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.



APPENDIX A

30.5 Logic testing.

Fault coverage measurement of manufacturing logic tests, test method 5012 of MIL-STD-883.

40. APPLICABLE DOCUMENTS

40.1 Government specification and standard. Unless otherwise specified, the following specification, and standard of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

STANDARD

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

40.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence.

50. REQUIREMENTS

50.1 Item requirements. The individual item requirements shall be in accordance with MIL-I-38535 and as specified herein.

50.2 Electrical test requirements. The electrical test requirements shall be in accordance with table 11 herein. The electrical tests for each subgroup are defined in table 1 herein.

50.3 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be in accordance with MIL-I-38535 and described herein.

50.3.1 Terminal connections. The terminal connections shall be as specified on figure 1 herein.

50.3.2 Truth table. The truth table (if applicable) shall be as specified on figure 2 herein.

50.3.3 Functional description. Figure 3 shall provide a brief description of the device function (block diagrams are recommended).

50.3.4 Case outline. The case outline shall be in accordance with 30.2.2 herein and as specified on figure 4.

50.3.5 Burn-in circuit. The device burn-in circuit shall be as specified on figure 5.

50.3.6 Radiation exposure circuit (when applicable). The radiation exposure circuit shall be as specified on figure 6.

50.4 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table 1 and apply over the full operating temperature range.

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## APPENDIX A

50.4.1 RHA environments (when applicable). PIPL and delta limits (when applicable) shall be specified in table I for the specified RHA environments.

50.5 Marking. Marking shall be in accordance with MIL-I-38535.

### 60. QUALITY ASSURANCE PROVISIONS

60.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-I-38535.

60.2 Screening. Screening shall be in accordance with MIL-I-38535 and shall be conducted on all devices.

60.2.1 Value added screens. Any value added screen beyond the requirements of MIL-I-38535 shall be detailed in table III.

60.3 Technology conformance inspections. Technology conformance inspections shall be in accordance with MIL-I-38535.

### 70. PACKAGING

70.1 Packaging requirements. The requirement for packaging shall be in accordance with MIL-I-38535.

### 80. NOTES

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions Temperature Range, RHA Environment	Group A Subgroups	Limits		Unit
				Min	Max	

List specific tests with parameters.

TABLE II. Electrical test requirements.

Test requirements	Subgroups
Interim electrical parameters Final electrical test parameters Group A test requirements Group C and D end-point electricals	In accordance with MIL-I-38535 and the device procurement specification

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## APPENDIX A

TABLE III. Value added screens.

Test	Requirements
List tests	As appropriate in accordance with Appendix B of MIL-I-38535

- Figure 1. Terminal connections
- Figure 2. Truth table
- Figure 3. Functional description
- Figure 4. Package outline
- Figure 5. Burn-in circuit
- Figure 6. Radiation exposure circuit

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APPENDIX B

SPACE APPLICATION

10. SCOPE

10.1 Scope. This appendix presents the requirements which shall be used to supplement MIL-I-38535 for space system microcircuits. This appendix is intended to be a transitional document.

10.2 Application. When specified by the procurement document (i.e., purchase order), the requirements of this appendix shall become a part of MIL-I-38535 and be implemented as specified herein.

20. APPLICABLE DOCUMENTS

20.1 Government documents.

20.1.1 Specifications and standards. The following specifications and standards form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents shall be those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation.

STANDARD

MILITARY

MIL-STD-454 - Standard General Requirements for Electronic Equipment.

30. REQUIREMENTS

30.1 General. Microcircuits supplied to this document shall be manufactured and tested in accordance with approved baselines and the requirements herein. The TRB shall not make major changes to the baselined processes, procedures, or testing without notifying the qualifying activity prior to implementation of the change for the device procurement specification in question.

30.1.1 Acquiring activity. When specified by the procurement document, the acquiring activity may:

- a. Require prior notification of major changes to the baselined processes, procedures, or testing.
- b. Require independent verification of wafers (unprobed) or packaged devices (TCV, SEC, or actual devices) by OEMs or Government agencies.
- c. Request screening and TCI summary data be delivered with the devices.

30.2 Conflicting requirements. In the event of conflict between the requirements of this appendix and other referenced documents, the order of precedence shall be as follows:

- a. The acquisition document (purchase order).
- b. Applicable device procurement specification.
- c. This appendix.
- d. MIL-I-38535.
- e. Specifications, standards, and other documents referenced in 2.1 of MIL-I-38535.

NOTE: The acquisition document may specify additional requirements, but shall not reduce or waive any requirements.

**30.3 Validation (certification).** Validation of a manufacturing line for production of integrated circuits for use in space systems shall be accomplished by a team which includes representatives for NASA and the Air Force Space Systems Division, in addition to the normal participation by DESC and RADC.

**30.4 Manufacturing verification.** When specified, the manufacturing verification procedure for new microcircuits shall include characterization of actual devices in increments of ambient or case temperature, supply voltage and input voltage levels over the specified parameter range.

**30.5 Design verification.** When specified, a descriptive model (i.e., VHDL), and a test vector set (i.e., tester independent support software system (TISSS) program) shall be available for independent verification of microcircuits in accordance with MIL-STD-454 Requirement 64.

**30.6 Part number.** When this appendix is imposed by contract or purchase order, a "V" mark shall be used in place of the "Q" mark in the part number format in 3.7.2.

#### 40. QUALITY AND RELIABILITY ASSURANCE

**40.1 Screening.** In addition to the screening tests specified in MIL-I-38535, the value added screening tests specified below shall be performed:

- a. Nondestructive bond pull (NDBP) in accordance with MIL-STD-883, test method 2023, or approved alternate verified during validation, on each interconnect bond. An alternate method, if necessary, shall consider a 100 percent visual inspection of the elements to be bonded (i.e., bond pads and posts) prior to the bonding operation.
- b. Internal visual inspection in accordance with MIL-STD-883, test method 2010, condition A, or approved alternate verified during validation on each microcircuit. An alternate method, if necessary, must address all the inspection topics of test method 2010.
- c. Particle impact noise detection (PIND) in accordance with MIL-STD-883, test method 2020 on each device.
- d. Reverse bias burn-in in accordance with MIL-STD-883, test method 1015 on each device when specified in the device procurement specification.
- e. Radiograph inspection in accordance with MIL-STD-883, test method 2012 on each device.
- f. Burn-in test in accordance with MIL-STD-883, test method 1015 on each device for 240 total hours at +125°C.

**40.2 Technology conformance inspection (TCI).** The TCI requirements listed below apply on each lot of deliverable devices. The group and table references correspond to those contained in MIL-I-38535. These requirements do not replace the normal TCI testing requirements of MIL-I-38535.

- a. Group A, table III, shall be performed on actual devices. For those lots having a quantity of less than 116 devices, the tests shall be imposed as 100 percent screens and the lot accepted on zero test rejects.

APPENDIX B

- b. Group B, table IV, shall be performed on actual devices. Dummy packages or reject devices may be used if it can be determined by the TRB that the intent of the test is not violated. The sample size of table IV is acceptable provided the 22(0) bond strength and solderability criteria has been applied to at least two separate devices (i.e., 11 leads per device), and the die shear test is applied with a 2(0) criteria.
- c. Group C, table V, shall be performed on a quantity(accept) criteria of 22(0). For lots greater than 200, actual devices shall be used. For lots less than or equal to 200, the number of actual devices shall be the greater of 5 devices or 10 percent of the lot, and the SEC shall supplement actual devices to result in a sample of 22.
- d. Group D, table VI, shall be performed on actual devices. Subgroup tests 2a, 3a, b, c, 4a, b, c, 5a, 6a, 7a, and 8a may be accomplished on dummy packages or rejected devices if it can be determined by the TRB that the intent of the test is not violated. The sample size (accept criteria) for group D lot tests shall be a minimum of 2(0) except that lead related tests shall be applied on a 22(0) basis, to at least two separate devices (i.e., 11 leads per device).

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CONCLUDING MATERIAL

Custodians:

Army - ER  
Navy - EC  
Air Force - 17  
NASA - NA

Preparing activity:

Air Force - 17

Agent:

DLA - ES

Review activities:

Army - AR, MI, PA  
Navy - MC  
Air Force - 11, 19, 85, 99  
DLA - ES

(Project 5962-1194)

User activities:

Army - SM  
Navy - AS, CG, OS, SH

Civil agency coordinating activity:

DOT-FAA(RD-650)

# STANDARDIZATION DOCUMENT IMPROVEMENT PROPOSAL

(See Instructions - Reverse Side)

1. DOCUMENT NUMBER MIL-I-38535		2. DOCUMENT TITLE MILITARY SPECIFICATION INTEGRATED CIRCUITS (MICROCIRCUITS) MANUFACTURING, GENERAL SPECIFICATION FOR	
3a. NAME OF SUBMITTING ORGANIZATION		4. TYPE OF ORGANIZATION (Mark one)	
		<input type="checkbox"/> VENDOR <input type="checkbox"/> USER <input type="checkbox"/> MANUFACTURER <input type="checkbox"/> OTHER (Specify): _____	
b. ADDRESS (Street, City, State, ZIP Code)			
5. PROBLEM AREAS			
a. Paragraph Number and Wording:			
b. Recommended Wording:			
c. Reason/Rationale for Recommendation:			
6. REMARKS			
7a. NAME OF SUBMITTER (Last, First, MI) - Optional		b. WORK TELEPHONE NUMBER (Include Area Code) - Optional	
c. MAILING ADDRESS (Street, City, State, ZIP Code) - Optional		8. DATE OF SUBMISSION (YYMMDD)	

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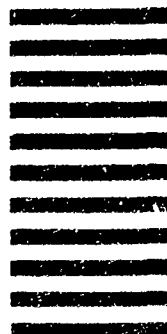
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## Appendix B

### Proposed Test Methods for VHSIC/VLSI Generic Qualification

06 JULY 1987

PROPOSED TEST METHOD 30XX  
MINIMUM PULSE WIDTH MEASUREMENT

1. PURPOSE. This method establishes the means for measuring the minimum clock pulse width requirements of microelectronic devices incorporating synchronous digital storage elements implemented in TTL, DTL, RTL, ECL and MOS.

1.1 Definitions. The following definitions shall apply to this test method.

1.1.1 Minimum Pulse Width (PW). That minimum amount of time (as measured at the specified reference voltages) separating the rising and falling edges of a square clock waveform which results in correct device response during execution of a functional test.

2. APPARATUS. Measurement of pulse widths requires equipment capable of:

- a) performing functional tests at a specified frequency from specified test vectors.
- b) generating clock signal pulses of variable width between specified low and high voltage levels with known input driver transition times.
- c) maintaining the device at the stated test temperature.

3. PROCEDURE. The driving signals shall be applied as specified in Method 3001 of this standard. The device under test shall be loaded according to Method 3002 of this standard. The device shall be stabilized at the specified test temperature.

3.1 Measurement of minimum pulse width (PW).

- a) The device under test shall be conditioned according to the applicable procurement document with nominal bias voltages applied.
- b) The data and clock low input levels used shall be at most their nominal low values. The data and clock high input levels used shall be at least their nominal high values.
- c) The minimum clock pulse width is determined through repeated application of a specified set of functional test vectors. A pass/fail bound of the clock pulse width is established by incrementally decreasing the pulse width with each successive functional test run.

### 3.1 Measurement of PW continued.

- d) The reported minimum clock pulse width will be the smallest pulse width which passes the functional test.
- \* e) The pulse width tests may be limited by the ability of the test equipment to generate narrow pulses. Should the device remain functional down to the equipment limits, the tester limits shall be reported.
- f) The device shall be assumed functional for all pulse widths greater than PW that do not exceed the maximum rated clock duty cycle.
- g) Minimum pulse width measurement may be reported as a minimum clock duty cycle percentage along with the associated clock frequency.

4. SUMMARY. The following details shall be specified in the applicable procurement document. See figure 30PW-1.

- a) The minimum clock pulse width pass/fail test limits.
- b) Vc<sub>ref</sub>: Clock pulse reference voltage.
- c) VIL<sub>c</sub>, VIH<sub>c</sub>: Clock low and high input levels.
- d) The rise and fall times of the clock driver waveform.
- e) VIL, VIH: low and high input levels for non-clock pins if different than those used for the clock waveform.
- f) The speed at which the functional test pattern is run.
- g) The power supply voltages.
- h) The test temperature.

#### \* EXPLANATION OF PROCEDURE ITEM 3.1e.

Item 3.1e of the pulse width test method described above is deemed necessary due to the finite rise and fall times associated with the driver circuitry of current generation ATE systems. Much commercially available VLSI ATE is incapable of generating squared-edged clock pulses of sufficient amplitude having widths less than 5-10 ns. Figure 30PW-2 shows a typical ATE driver response when the programmed pulse width is small compared to the rise and fall times.

## MINIMUM PULSE WIDTH MEASUREMENT

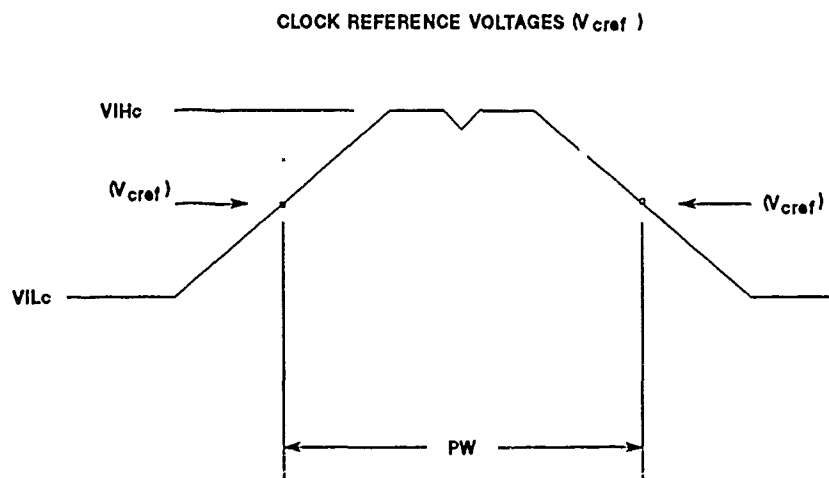
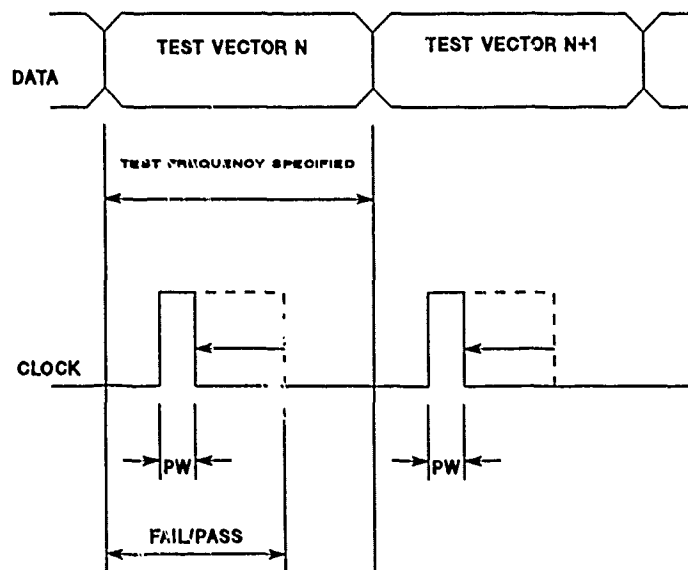
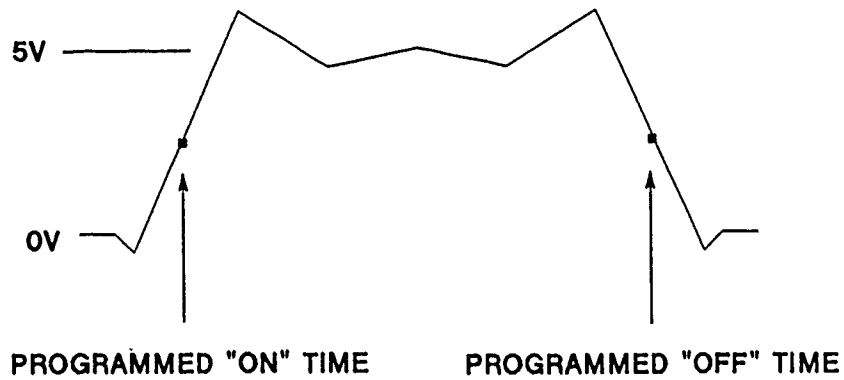
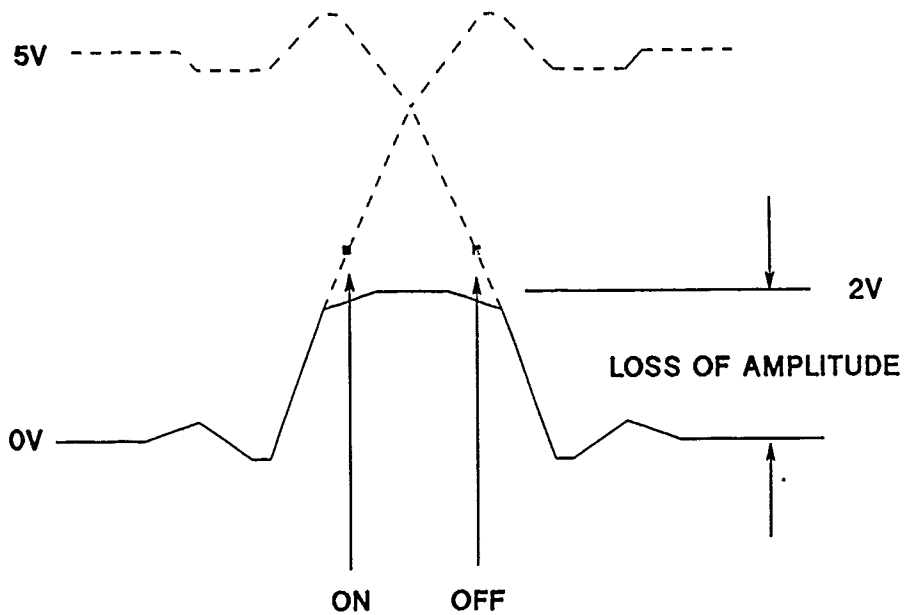


FIGURE 30PW-1

## POOR NARROW PULSE



A 5V 10NS PULSE



A 5V 2NS PULSE

FIGURE 30PW-2

10 JULY 1987

ADDENDUM TO TEST METHOD 3005

DYNAMIC POWER DISSIPATION

1. PURPOSE. This method establishes the means for calculating the dynamic power consumption of digital logic circuits from dynamic power supply current measurements. Some test issues concerning MOS devices are presented.

1.1 Definitions. The following definitions shall apply to this test method.

1.1.1 Dynamic Power Supply Current ( $I_{dd}, I_{ss}, I_{cc}, I_{ee}$ ). The average current measured at the power supply terminals while the device is stimulated by a functional test pattern.

1.1.2 Dynamic Power Dissipation ( $P_{av}$ ). The average power consumed by the device during operation.

2. CALCULATION OF DYNAMIC POWER DISSIPATION ( $P_{av}$ ). The dynamic power dissipation is computed from average current measurements as:

$$P_{av} = I_{av} * V$$

where  $I_{av}$  is the average measured power supply current ( $I_{dd}, I_{ss}, I_{cc}$  or  $I_{ee}$ ).  
 $V$  is the power supply voltage at which the current is measured.

3. COMMENTS ON MEASURING AVERAGE CURRENT AND POWER.

- a) Large capacitors should be used on the test fixture to eliminate potentially large current spikes resulting from switching transients. Adequate filtering should be verified prior to making the current measurement by observing the power supply voltage on an oscilloscope while the functional test is performed.
- b) Average power supply current can be measured with analog or digital instrumentation if it properly averages glitchy, non-sinusoidal waveforms should they exist.

- c) The dynamic power consumption of MOS devices is substantially larger than their static power consumption. This is especially true for CMOS devices where almost all power dissipation occurs only during node switching. The power consumed by MOS devices is directly proportional to the test vector frequency and the degree of node activity associated with the particular functional test employed. Consequently, the measured power dissipation of MOS devices may be a strong function of the test vectors used.
- d) A substantial percentage of the dynamic power dissipation of small geometry devices typically lies in the chip's output buffer circuits and the load to which these pins are attached.
- e) The power dissipation measurement should be made under worst case temperature, loading, power supply voltage and test vector conditions.

4. SUMMARY. The following details shall be specified in the applicable procurement document.

- a) The maximum allowable power dissipation.
- b) The power supply and input voltages used.
- c) The load seen by the output pins.
- c) The speed at which the functional test pattern is run.
- d) The test temperature.



06 JULY 1987

REVISED TEST METHOD 3007

LOW LEVEL OUTPUT VOLTAGE MEASUREMENT

1. PURPOSE. This method establishes the means for measuring the steady state low level output voltage of TTL, DTL, RTL, and MOS microelectronic devices under controlled worst case power supply and loading conditions.

1.1 Definitions. The following definitions shall apply to this test method.

1.1.1 Low Level Output Voltage (VOL). The dc low level output voltage measured at the device output pins under worst case power supply and current loading conditions. Worst case VOL conditions are defined as those rated power supply voltages which result in the highest measured output voltage and the use of the largest positive current loading allowed by the rated device fanout.

1.2 Load Current (IOL) Sign Convention. Positive load current will represent conventional current flow out of the test equipment and into the device output terminal. Negative load current will represent conventional current flow out of the device terminal into the test equipment.

2. APPARATUS. Measurement of low output voltage requires equipment capable of:

- a) providing the worst case power supply voltages and applying worst case load currents (IOL) to the pins under test.
- b) executing a specified group of initialization test vectors which place the required output nodes in a logical low state.
- c) measuring the pin dc output voltage.
- d) maintaining the device at the stated test temperature.

3. PROCEDURE. The driving signals shall be applied as specified in Method 3001 of this standard. The device under test shall be loaded according to Method 3002 of this standard. The device shall be stabilized at the specified test temperature.

3.1 Measurement of low output voltage (VOL).

- a) The device under test shall be conditioned according to the applicable procurement document using worst case power supply voltages.
- b) A specified group of initialization test vectors shall be applied to establish logical low levels at the required output pins.
- c) The specified worst case load current shall be applied.

3.1 VOL Procedure Continued. `

- d) Sufficient time will be allowed to guarantee steady state conditions at the output pins.
- e) The output pin voltage is measured.

4. SUMMARY. The following details shall be specified in the applicable procurement document.

- a) The VOL pass/fail test limits.
- b) The worst case power supply voltages used.
- c) The value of the worst case load current applied to the output pins.
- d) The test temperature.

06 JULY 1987

REVISED TEST METHOD 3006

HIGH LEVEL OUTPUT VOLTAGE MEASUREMENT

1. PURPOSE. This method establishes the means for measuring the steady state high level output voltage of TTL, DTL, RTL, and MOS microelectronic devices under controlled worst case power supply and pin loading conditions.

1.1 Definitions. The following definitions shall apply to this test method.

1.1.1 High Level Output Voltage (VOH). The dc high level output voltage measured at the device output pins under worst case power supply and current loading conditions. Worst case VOH conditions are defined as those rated power supply voltages which result in the lowest measured output voltage and the use of the largest negative current loading allowed by the rated device fanout.

1.2 Load Current (IOH) Sign Convention. Positive load current will represent conventional current flow out of the test equipment and into the device output terminal. Negative load current will represent conventional current flow out of the device terminal into the test equipment.

2. APPARATUS. Measurement of high output voltage requires equipment capable of:

- a) providing the worst case power supply voltages and applying worst case load currents (IOH) to the pins under test.
- b) executing a specified group of initialization test vectors which place the required output nodes in logical high states.
- c) measuring the pin dc output voltage.
- d) maintaining the device at the stated test temperature.

3. PROCEDURE. The driving signals shall be applied as specified in Method 3001 of this standard. The device under test shall be loaded according to Method 3002 of this standard. The device shall be stabilized at the specified test temperature.

3.1 Measurement of high output voltage (VOH).

- a) The device under test shall be conditioned according to the applicable procurement document using worst case power supply voltages.
- b) A specified group of initialization test vectors shall be applied to establish logical high levels at the required output pins.
- c) The specified worst case load current shall be applied.

3.1 VOH Procedure Continued.

- d) Sufficient time will be allowed to guarantee steady state conditions at the output pins.
- e) The output pin voltage is measured.

4. SUMMARY. The following details shall be specified in the applicable procurement document.

- a) The VOH pass/fail test limits.
- b) The worst case power supply voltages used.
- c) The value of the worst case load current applied to the output pins.
- d) The test temperature.

13 JULY 1987

PROPOSED TEST METHOD 30XX

WAFER PROBE CONTACT TEST

1. PURPOSE. This method establishes the means for verifying probe card to bonding pad contact for TTL, DTL, RTL, ECL and MOS microelectronic devices during wafer level testing.

1.1 Definitions. The following definitions shall apply to this test method.

1.1.0 Clamp Voltage. The maximum allowable probe voltage. A dc constant current test source applied to the device bonding pads will be clamped such that the probe voltage never exceeds the specified limiting clamp voltage.

1.1.1 Voltage Input Clamp (VIC). The voltage measured at an input pad during application of the continuity test described below.

1.1.2 Voltage Output Clamp (VOC). The voltage measured at an output pad during application of the continuity test described below.

1.1.3 VIC+, VIC-, VOC+, VOC-. The VIC and VOC voltage clamp tests may be further classified as plus or minus depending on the direction of forced test current flow. The plus tests (VIC+ and VOC+) utilize a positive test current which is defined as conventional current flow out of the test equipment and into the device pad. The minus tests (VIC- and VOC-) draw conventional current flow out of the device pad and into the test equipment.

2. GENERAL DESCRIPTION. The VIC and VOC tests are a check of electrical continuity between the test head electronics, the probe card interface, the device under test and a return path to the test equipment via chip power supply and ground connections. Any additional test fixturing appearing in this loop is also verified. The method described herein requires that a low resistance path to ground or a device power supply terminal be available either by direct internal connection or through forward biased pn junctions. This path will typically appear in the chip buffer circuitry or in on-chip electrostatic protection structures. The test for continuity is made by applying a dc constant current source to the input and/or output pads on an individual basis and measuring the probe voltage. Open circuits will register a voltage equal to or near the specified voltage clamp limit. The on-chip path to a known potential must therefore provide a dc resistance to current flow which is low enough to distinguish the associated voltage drop across this path from an open circuit.

The specified values of forced test current and source clamp voltage should be low enough to protect both the device and the small probe contact points. Although the VIC and VOC tests are essential during wafer level electrical test where probe positioning is of concern, the same technique is equally suitable for verifying the tester/device interface of packaged parts. The VIC and VOC continuity checks are typically performed before any other electrical test and a VIC/VOC failure will normally preclude any additional testing of the device. Establishing the required low resistance path may involve a unique chip set-up (such as grounded power supplies) which is not encountered in normal device operation. The VIC and VOC tests should be performed at every temperature during temperature cycling as icing and thermal stresses can substantially degrade points of mechanical contact.

2. APPARATUS. Measurement of VIC and VOC requires equipment capable of:

- a) forcing a specified dc test current into or out of the device bonding pads subject to a specified limiting probe clamp voltage.
- b) measuring the probe voltage while the dc test current is applied.
- c) maintaining the device at the stated test temperature.

3. PROCEDURE. The driving signals shall be applied as specified in Method 3001 of this standard. The device under test shall be loaded according to Method 3002 of this standard. The device shall be stabilized at the specified test temperature.

3.1 Measurement of VIC or VOC.

- a) The device under test shall be conditioned according to the applicable procurement document with the specified power supply voltages.
- b) The specified dc test current will be applied to the device bonding pads through the probe card interface.
- c) The probe voltage (VIC or VOC) is measured while the test current is applied.
- d) A pass or fail decision is made based on the measured probe voltage.

4. SUMMARY. The following details shall be specified in the applicable procurement document.

- a) The VIC and VOC pass/fail test limits.
- b) The power supply voltages.
- c) The treatment of pins not currently being tested.
- d) The amount of test current to be forced on the device pad.
- e) The current source clamp voltage.
- f) The test temperature.

25 MARCH 1987

METHOD 30TS.1

# HOLD TIME MEASUREMENTS

1. PURPOSE. This method establishes the means for measuring the hold time of microelectronic devices incorporating synchronous digital storage elements implemented in TTL, DTL, RTL, ECL and MOS.

1.1 Definitions. The following definitions shall apply to this test method.

1.1.1 Active clock edge. That transition of the input clock signal which causes valid data applied at the input pins to be stored in a flip-flop, latch or comparable digital memory element.

1.1.2 Valid data. That voltage representing a logical 0 or 1 which is to be stored in the memory element.

1.1.3 Hold time (tH). That minimum amount of time (as measured at the specified reference voltages) that valid data must be maintained after the active clock edge. The symbol tH will imply that the reported value represents the worst case (most positive) result of tHL and tHH tests.

1.1.3.1 Hold time for low input data (tHL). The symbol tHL will imply that the valid data to be stored is a logical 0.

1.1.3.2 Set-up time for high input data (tHH). The symbol tHH will imply that the valid data to be stored is a logical 1.

1.1.3.3 Positive hold time. A positive value of hold time will imply that the data to be stored must be maintained at the input pins for at least tH seconds after the active clock edge.

1.1.3.4 Negative hold time. A negative value of hold time will imply that the data to be stored may be removed from the input pins at most tH seconds before the active clock edge. Hold times which measure negative may be reported as 0.0 seconds.

2. APPARATUS. Measurement of hold time requires equipment capable of:

- a) generating input data and clock signal transitions between specified low and high levels within a specified transition time.
- b) skewing data and clock input waveforms relative to each other.
- c) measuring the time difference between the data and clock input waveforms at specified reference voltages.
- d) detecting the logical value of the data stored.
- e) maintaining the device at the stated test temperature.

3. PROCEDURE. The driving signals shall be applied as specified in Method 3001 of this standard. The device under test shall be loaded according to Method 3002 of this standard. The device shall be stabilized at the specified test temperature.

3.1 Measurement of hold time.

- a) The device under test shall be conditioned according to the applicable procurement document with nominal bias voltages applied.
- b) The data and clock low input levels used shall be at most their nominal low values. The data and clock high input levels used shall be at least their nominal high values.
- c) During the execution of the hold time measurement all data input pins will be allowed a set-up time which is sufficient to guarantee accurate generation of the data waveform.
- d) A pass/fail bound of the relative timing of data and clock signals is established by incrementally skewing these input waveforms relative to each other.
- e) The hold time is computed from time measurements shown in Figure 30TH-1.

4. SUMMARY. The following details shall be specified in the applicable procurement document.

- a) The hold time pass/fail test limits.
- b) The following voltages as shown in Figure 30TH-1:
  - Vcref: Clock input reference voltage.
  - Vdref: Data input reference voltage.
  - VILc, VILd: Clock and Data low input levels.
  - VIHc, VIHd: Clock and Data high input levels.
- c) The rise/fall time parameters of the clock and data input driver waveforms.
- d) The logical value of valid data used if applicable.
- e) The power supply voltages.
- f) The test temperature.



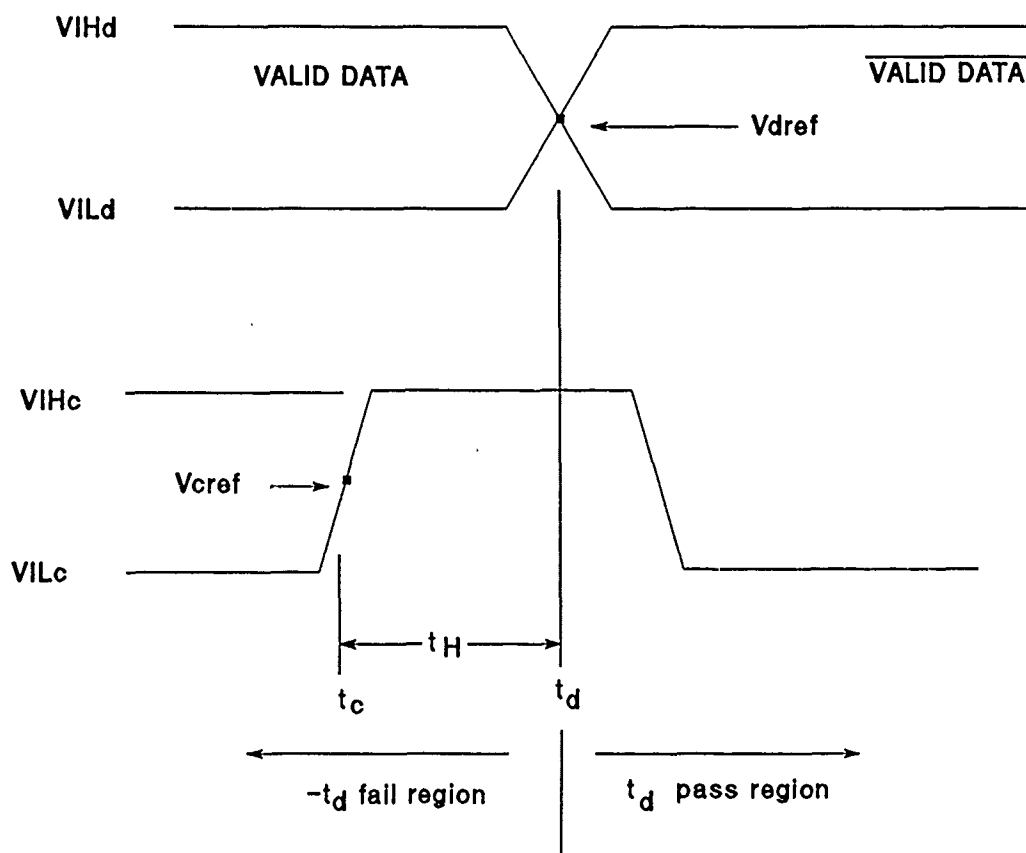
ADDITIONAL DEFINITIONS PERTAINING TO FIGURE 30TH-1  
FOR THE MEASUREMENT OF HOLD TIME

- Vc<sub>ref</sub>. The clock reference voltage used to fix t<sub>c</sub>.  
Vc<sub>ref</sub> to be specified in applicable procurement document.
- Vd<sub>ref</sub>. The data reference voltage used to fix t<sub>d</sub>.  
Vd<sub>ref</sub> to be specified in applicable procurement document.
- t<sub>c</sub>. The time at which the clock input signal crosses Vc<sub>ref</sub> volts in an active transition.
- t<sub>d</sub>. The time at which the data input signal crosses Vd<sub>ref</sub> volts in its transition from valid data to the complement of valid data.
- VIL<sub>c</sub> & VIL<sub>d</sub>. Steady state clock and data low input voltages.  
To be specified in applicable procurement document.
- VIH<sub>c</sub> & VIH<sub>d</sub>. Steady state clock and data high input voltages.  
To be specified in applicable procurement document.
- t<sub>d</sub> pass region. Valid data is correctly stored whenever it is maintained at the input terminals for times greater than or equal to t<sub>d</sub>.
- t<sub>d</sub> fail region. Valid data is not correctly stored whenever it is removed from the input terminals at times less than t<sub>d</sub>.
- t<sub>H</sub>. Using the above definitions of clock time (t<sub>c</sub>) and valid data time (t<sub>d</sub>) the hold time is given by:

$$\text{HOLD TIME: } t_H = t_c - t_d.$$

# HOLD TIME MEASUREMENTS

SHOWN: RISING EDGE ACTIVE CLOCK WITH POSITIVE HOLD TIME



$$\text{HOLD TIME: } t_H = t_d - t_c$$

FIGURE 30TH-1

Task Number 1317

25 MARCH 1987

METHOD 30TS.1

SET-UP TIME MEASUREMENTS

1. PURPOSE. This method establishes the means for measuring the set-up time of microelectronic devices incorporating synchronous digital storage elements implemented in TTL, DTL, RTL, ECL and MOS.

1.1 Definitions. The following definitions shall apply to this test method.

1.1.1 Active clock edge. That transition of the input clock signal which causes valid data applied at the input pins to be stored in a flip-flop, latch or comparable digital memory element.

1.1.2 Valid data. That voltage representing a logical 0 or 1 which is to be stored in the memory element.

1.1.3 Set-up time ( $t_S$ ). That minimum amount of time (as measured at the specified reference voltages) by which the transition to valid data must precede the active clock edge. The symbol  $t_S$  will imply that the reported value represents the worst case (most positive) result of  $t_{SL}$  and  $t_{SH}$  tests.

1.1.3.1 Set-up time for low input data ( $t_{SL}$ ). The symbol  $t_{SL}$  will imply that the valid data to be stored is a logical 0.

1.1.3.2 Set-up time for high input data ( $t_{SH}$ ). The symbol  $t_{SH}$  will imply that the valid data to be stored is a logical 1.

1.1.3.3 Positive set-up time. A positive value of set-up time will imply that the transition to valid data must precede the active clock edge by at least  $t_S$  seconds for proper storage.

1.1.3.4 Negative set-up time. A negative value of set-up time will imply that the transition to valid data may trail the active clock edge by at most  $t_S$  seconds for proper storage. Set-up times which measure negative may be reported as 0.0 seconds.

2. APPARATUS. Measurement of set-up time requires equipment capable of:

- a) generating input data and clock signal transitions between specified low and high levels within a specified transition time.
- b) skewing data and clock input waveforms relative to each other.
- c) measuring the time difference between the data and clock input waveforms at specified reference voltages.
- d) detecting the logical value of the data stored.
- e) maintaining the device at the stated test temperature.

3. PROCEDURE. The driving signals shall be applied as specified in Method 3001 of this standard. The device under test shall be loaded according to Method 3002 of this standard. The device shall be stabilized at the specified test temperature.

3.1 Measurement of set-up time.

- a) The device under test shall be conditioned according to the applicable procurement document with nominal bias voltages applied.
- b) The data and clock low input levels used shall be at most their nominal low values. The data and clock high input levels used shall be at least their nominal high values.
- c) During the execution of the set-up time measurement all data input pins will be allowed a hold time which is sufficient to guarantee accurate generation of the data waveform.
- d) A pass/fail bound of the relative timing of data and clock signals is established by incrementally skewing these input waveforms relative to each other.
- e) The set-up time is computed from time measurements shown in Figure 30TS-1.

4. SUMMARY. The following details shall be specified in the applicable procurement document.

- a) The set-up time pass/fail test limits.
- b) The following voltages as shown in Figure 30TS-1:
  - V<sub>c</sub>ref: Clock input reference voltage.
  - V<sub>d</sub>ref: Data input reference voltage.
  - V<sub>ILc</sub>, V<sub>ILd</sub>: Clock and Data low input levels.
  - V<sub>IHc</sub>, V<sub>IHd</sub>: Clock and Data high input levels.
- c) The rise/fall time parameters of the clock and data input driver waveforms.
- d) The logical value of valid data used if applicable.
- e) The power supply voltages.
- f) The test temperature.

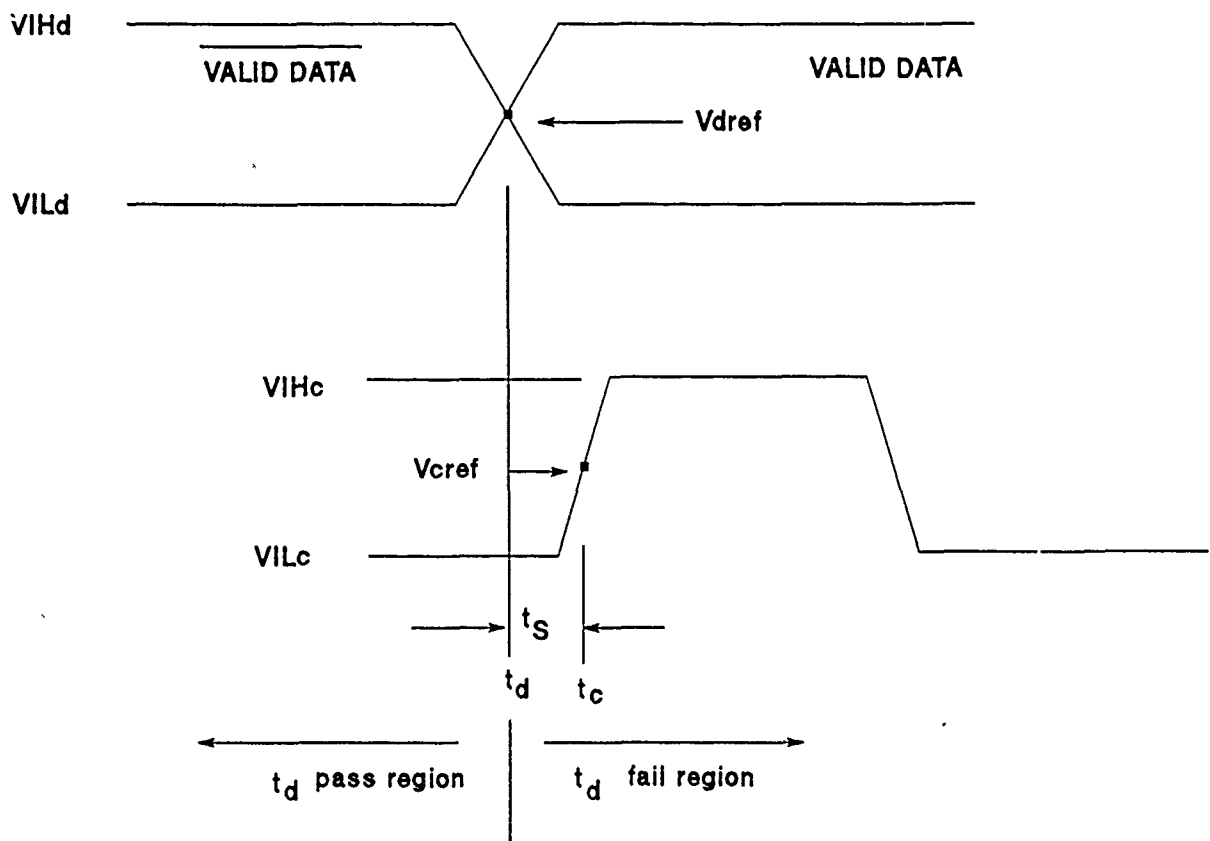
ADDITIONAL DEFINITIONS PERTAINING TO FIGURE 30TS-1  
FOR THE MEASUREMENT OF SET-UP TIME

- V<sub>cref</sub>. The clock reference voltage used to fix t<sub>c</sub>.  
V<sub>cref</sub> to be specified in applicable procurement document.
- V<sub>dref</sub>. The data reference voltage used to fix t<sub>d</sub>.  
V<sub>dref</sub> to be specified in applicable procurement document.
- t<sub>c</sub>. The time at which the clock input signal crosses V<sub>cref</sub> volts in an active transition.
- t<sub>d</sub>. The time at which the data input signal crosses V<sub>dref</sub> volts in its transition from the complement of valid data to valid data.
- V<sub>ILc</sub> & V<sub>ILd</sub>. Steady state clock and data low input voltages.  
To be specified in applicable procurement document.
- V<sub>IHc</sub> & V<sub>IHd</sub>. Steady state clock and data high input voltages.  
To be specified in applicable procurement document.
- t<sub>d</sub> pass region. Valid data is correctly stored whenever it is established at the input terminals at times less than or equal to t<sub>d</sub>.
- t<sub>d</sub> fail region. Valid data is not correctly stored whenever it is established at the input terminals at times greater than t<sub>d</sub>.
- t<sub>S</sub>. Using the above definitions of clock time (t<sub>c</sub>) and valid data time (t<sub>d</sub>) the set-up time is given by:

$$\text{SET-UP TIME: } t_S = t_c - t_d.$$

## SET-UP TIME MEASUREMENTS

SHOWN: RISING EDGE ACTIVE CLOCK WITH POSITIVE HOLD TIME



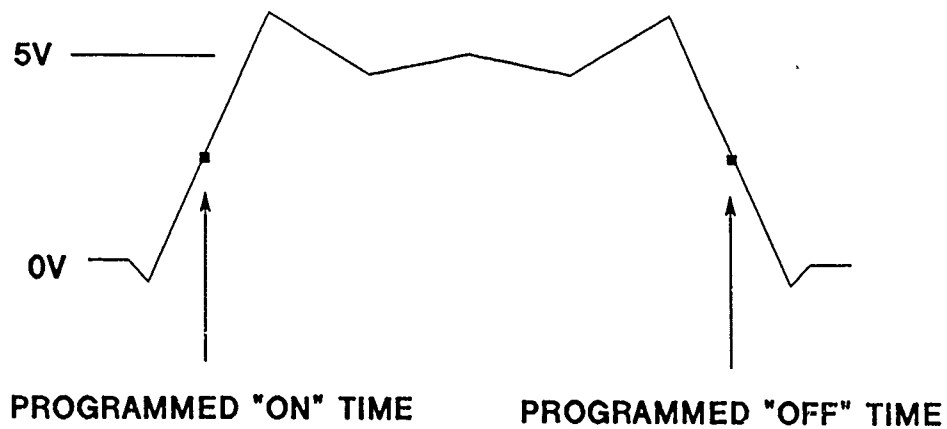
$$\text{HOLD TIME: } t_s = t_c - t_d$$

FIGURE 30TS-1

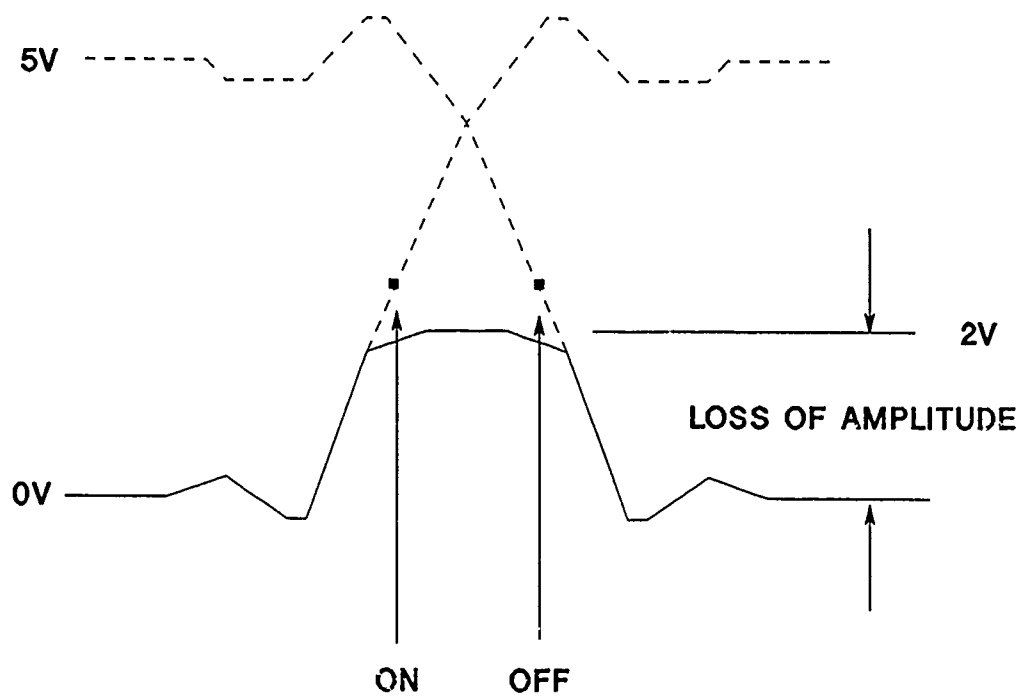
EXPLANATION OF SET-UP AND HOLD METHODS  
ITEM 3.1C

Item 3.1c under the proposed set-up and hold testing methods is deemed necessary due to the finite rise and fall times associated with the driver circuitry of current generation ATE systems. Consider a hypothetical flip-flop with known set-up time of 0.5ns and hold time of 1.0ns. Such a device requires only that the desired data be available at the input pin during a 1.5ns pulse properly centered about the active clock edge. Commercially available VLSI ATE is incapable of generating such a narrow pulse. Test method item 3.1c is therefore included to circumvent this constraint on minimum pulse width. A direct consequence of this provision is that set-up and hold tests are not required to be performed simultaneously.

The figure on the next page shows a typical driver response to a pulse width that has been set too small.



A 5V 10NS PULSE



A 5V 2NS PULSE

FIGURE 30PW-3



## Appendix C

### Proposed Requirements to Qualify CAD Tools for VHSIC/VLSI Devices

## 1. Generic Plan

This Qualification plan is applicable to all software Computer Aided Developmental(CAD) tools used in the VHSIC design process being Qualified. Since, all CAD Tools covered in this Qualification Plan are used in the design methodology of VHSIC devices and the Design Organization controls the design methodology, the control of CAD Tools is placed with the Design Organization.

This plan treats each tool as a Black Box, i.e., the major interest is input to the tool and output from the tool. How the tool processes the input to produce its output is of minor concern. Any major deviation from this philosophy would greatly inhibit the development and placement of new and improved tools and would not allow for differences in the environment of the various VHSIC Processes. Also the Black Box methodology will reduce the reluctance of a tool's vendor to qualify for propriety reasons, reduce the knowledge needed to qualify a tool and reduce the time to qualify a tool.

## 2. Steps to Qualify CAD Tools

1. A CAD Tool List must be submitted to the Qualifying Organization.
2. A Tool Function List must be submitted to the Qualifying Organization for each Qualifying Tool.
3. A Tool Dependency List must be submitted to the Qualifying Organization for each Qualifying Tool.
4. A Qualification Plan must be developed for each Tool and submitted to the Qualifying Organization.
5. Each Tool must meet the Qualification objectives stated in its Qualification Plan.
6. The Archiving Facility must be Qualified.

## 3. CAD Tool List

It is the Design Organizations responsibility to prepare a complete list of all CAD tools used in the VHSIC facility to be qualified, the *CAD Tool List*. It is assumed that the overall responsibility for the VHSIC design and production will reside with the Design Organization and the owner of the VHSIC production facilities will be considered as a sub\_contractor. This list shall include:

1. the tool name.

2. the version currently being used,
3. the date this version was installed,
4. the identity of the installer,
5. the date the tool was qualified,
6. a short description of the tools purpose,
7. tool sponsor.

Each tool must have a sponsor, a person who is responsible for the tool in the Design Organizations facility. The name of the tool's sponsor must be entered on the *CAD Tool List*. The *CAD Tool List* must be available to the Qualifying personnel before Qualification begins. If a tool has not been Qualified, then the qualification date is blank.

As a new version of the tool is installed for execution, the following must be added to the *CAD Tool List*:

1. the tool name,
2. the version number,
3. the date of installation,
4. the identity of the installer
5. the date the version is Qualified,
6. the tool sponsor.

If a tool has not been Qualified, then the qualification date is blank.

If a waiver has been granted for a Tool, then the following must be added to the *CAD Tool List*:

1. Tool name,
2. Tool version number.
3. Tool sponsor,
4. type of waiver (Reliability, Qualification or Archive Facility),
5. date waiver is approved,
6. date waiver expires,
7. name of the Qualification Organization person who approved the waiver,
8. a short reason for the waiver request.

All data on the *CAD Tool List* must be current.

#### 4. Tool Function List

Each Tool must have an official minimum set list of Functions, *Tool Function List*. For the purpose here, if a minimum function is omitted, then the user can not perform the job the tool was designed to do. Only minimal functions are included in the specification: i.e., the word function means minimal function for this document unless specified. It is the Design Organizations responsibility to produce and verify the *Tool Function List* for each tool. It is the responsibility of the vendor of the tool to provide methods to verify that each function operates as expected as described in the accompanying documentation of the tool (see Documentation). The *Tool Function List* must have:

1. Tool name,
2. version number,

3. Tool sponsor name,
  4. each Tool Function name,
  5. a short description of the function,
  6. date the function Qualified.
- If a Tool Function has not been Qualified, then the qualification date is blank.

The VHSIC design process cannot use any functions of a tool not on this official *Tool Function List* and not *Qualified*. The *Tool Function List* must be available to the Qualifying personnel.

## 5. CAD Tool Dependency List

A *Tool Dependency List* is a list of all Tools and the communication of data among Tools used in the VHSIC environment. Contents of the *CAD Tool Dependency List*:

1. Tool Name,
  2. version number,
  3. Tool sponsor,
  4. name of the Dependent Tool accepting input or output from this Tool,
  5. name of file(if applicable),
  6. type of file(input/output),
  7. a short description of the file, or
  8. if communication is data not in a file, then the data name(if applicable), data type(input/output) and a short description of the data is required.
- All Tools on the *CAD Tool List* must be on this list. If the Tool does not communicate to any other Tool, then the name of the Dependent Tool is "none".

## 6. Archive Facilities Qualification

The Archiving Facilities must be tested to insure that Archived material may be retrieved correctly and conveniently. To Qualify an Archive Facility:

1. A Journal from at least one of the Tools should be Archived and then Retrieved. The Retrieved Journal should playback through the Tool and the resulting activity should match the original journal session.
2. The Archive Facility should demonstrate long term archiving by retrieving and successfully executing files stored for at least 1, 2, 3 years. If this is not possible at the start of the first Qualification Inspection, then 3 months retrieval must be demonstrated and the longer term storage can be waived by Qualifying personnel. However, the 1, 2 and 3 year storage must be tested for the Qualifying personnel as the time expires and the waiver lifted at the end of successfully demonstrating 3 year retrieval. If an Archiving-waver is issued by the Qualifying personnel, then notification that the the waver was issued must be appended to the *CAD Tool List*.
3. An off-site alternate Archive storage site must exist to protect from local disasters. An Archived File stored at the alternate site must be retrieved and the retrieved file must be successfully executed. Long term off-site storage must be demonstrated as described above. Note, off-site implies another physical building at least 5 miles from the original site.

## 7. CAD Tool Qualification Plan

It is the Vendor of the tools responsibility to provide a detailed plan to demonstrate the correctness and capability of the tool, *CAD Tool Qualification Plan*. The plan should include the input to the tool, its output or action and methods of verifying the correctness of the output or action for each function on the *Tool Function List*. The capability of the tool must be demonstrated.

### 7.1 Vendor of the Tool

The Vendor of the tool is normally the organization or its representative who developed the software for the CAD Tool. However, the Design Organization has the ultimate responsibility of adhering to the *VHSIC CAD Tool Qualification Plan*. The word Design Organization may be substituted for the word Vendor throughout this document.

### 7.2 Verifying Correctness of a Tool Function

A Tool Function is considered correct when the documented input produces the desired results or actions, and further, the results or actions match those described in the documentation of the tool.

### 7.3 Demonstrating Capability of a Tool Function

A Tool Function has demonstrated Capability when it is able to process VHSIC circuits near the maximum complexity processed in the VHSIC Line being Qualified and when the time and cost of the processing is within the Industry norm for the Tool Function.

## 8. Tools Version Identity

The release version identity of the tool is the responsibility of the Vendor of the Tool. It is the Tool Vendors responsibility to designate major or minor changes to the tool. Each additional installation of the tool in the VHSIC facility other than a copy must have a new identifying version number. These version numbers should be in ascending sequence; major and minor version numbers must be identified.

### 8.1 Current Version

The current version of a tool is the version executing in the Qualified VHSIC facility and is used to develop the devices in the facility. Normally, this would be the last Qualified version listed on the *CAD Tool List*.

### 8.2 Compatibility of Software Release Versions

All subsequent versions of a software tool must accept the previous versions input. Version Compatibility. This should be part of the tool but may be furnished by a stand-alone software translation system. A new version of a tool should provide the critical functions of the previous version, and, a new version should accept and execute the Journal File (see Human Entry section) of the previous version. This provides a method of testing the accuracy of the new version to the standards of the previous version.

## 9. Tool Input

### 9.1 Human Entry

For each tool, all human entered data must be captured by the machine running the tool in a file or files that are saved or Archived (see Archive Files section). This Archived File or Files is called a

*Journal File* because it is a record of all human data entered during the session the tool was run. This Journal File must be formatted in a human readable or convertible to a human readable format via a machine resident translating system. Further, the tool must be able to read this archived data Journal in place of the human entry and execute the commands in the Journal File as if the commands were human entered, *Playback*. As new versions of the tool become available, this journaling and playback capability is used to qualify the new version against the standard of the old version. Note; the human readable requirement is designed to provide portability and thus not be dependent on hardware or versions of software(host operating system and/or the tools system).

## 9.2 Machine Entry

If a tool's input is from another tool, tool-to-tool communication, then the input must be verifiable and specifications exist describing its format. The responsibility to verify the correctness of the tool-to-tool communication resides with the vendor introducing the new version or tool. If tool A outputs data that tool B uses as input; then, if tool A introduces a new version or tool, the vendor of tool A is responsible for the verification. The reverse is also true; tool A output is input to tool B and vendor of tool B introduces a new version or tool, the vendor of tool B is responsible for verification that tool B correctly interprets the input from tool A. (See also *CAD Tool Dependency List* section.)

## 9.3 Tools Response to Data

The Tool's Software should produce good results for test data without aborting when an abort is not the desired result. When an abort is expected as part of the test data, then comprehensible error messages should be generated. All error messages should be understandable to a normal user of the tool.

## 9.4 Verification of Input

Verification of input requires that given the input meets documented standards, then, the tool reacts as expected judged against its documentation.

# 10. Tool Output

The output or action of each function in the tool must be verifiable, either by building the device and observing its operation or by capturing computer output and demonstrating its correctness or by entering documented input and observing the action against documented action. The vendor of the tool is responsible to provide methods to demonstrate the correctness of the output or action.

## 10.1 Output Format

A written specification must exist describing the format of all output that exists after a tools session is ended (permanent output). This includes data that is used by the tool to continue from session-to-session. The output must be capable of being archived and all environmental parameters affecting the operation of the tool, including date stamping, must be included in the archived file(see *Archive Files*). All archivable output must be in human readable form or a translator exist to convert the output to that form. An exception to the human readable condition can be made when the output is in an industry or government accepted standard format.

### 10.1.1 Archive Files

All Archived Files must be labeled so that all environmental parameters affecting the output or action of the tool may be identified(time, date, session, tool, tool version, Machine and Machine operating system, etc.). Archived Files imply that the files are stored for at least the length of the contract and may be retrieved within a reasonable time in the same state as when archived. The

Archiving Facilities must be Qualified.

## 11. Documentation

All supporting documentation must be complete and current with the tool's current version number and specify the version number being supported. It must specify the input and the expected action or output of all functions. All archivable output(non-temporary files) must be described in the documentation. A temporary file is one that only exists during the execution of the tool and need not be documented. To verify that documentation is correct, the documented input to a function is entered and the resulting output or action must match the description of the results recorded in the documentation. If the match does not occur, then either the software or documentation must be changed by the vendor before the Tool can be Qualified and the function must be Requalified. All functions must be Qualified; where this is not possible, then the percentage of coverage must be documented. The coverage must be equal or above industry norm for this VHSIC environment.

## 12. Testing Models

Where appropriate each software tool should be tested with a set of approved models of various sizes(cell, macro, subchip and chips of at least 2 sizes) to test each product for correctness and capability. One of the chips should be of small to moderate size to check correctness and the other should be a large chip, as bounded by the maximum size chip produced in the VHSIC facility, to check capability of the tool to process large jobs in reasonable time and cost. Reasonableness may be judged against Industry norms for this tool and function. Where models are not appropriate, then the vendor of the tool must provide a method to verify the output of the tool for correctness and capability(see Correctness and Capability sections).

## 13. Reliability or Quality Qualification

The reliability of the tool must be documented. The measure or Figure of Merit for Quality is the number of Severe Faults (see Severe Fault section) per 1000 lines of non-commented code. A Tool Qualifies for Quality by showing that the Quality Figure of Merit or some function of the Figure of Merit is either stable or decreasing in time using standard statistical methodology. This Figure of Merit should be below the median figure for all software released in the United States.

If a new version of the tool is released, then previous reliability data may be applied to the new release if the vendor of the tool has demonstrated reliability at revisions.

### 13.1 Severe Fault

#### 13.1.1 Fault

A Fault is a deviation of specified action from documented action given specified documented input.

#### 13.1.2 Severe Fault

A Severe Fault is a fault that prevents the user from performing the function or executing the tool for which there is no convenient work-around.

#### 13.1.3 Work-around

A work-around is a substitute set of actions or functions executing under the tool that executes a function working incorrectly or not working at all to produce correct results.

The standard cell symbols should correctly match the library symbols used in the VHSIC environment. The symbol layout displayed by the Tool should be true to the netlist produced by the Tool. Since the Schematic Capture System normally interacts with simulation and layout tools, then the netlist file should be tested for input compatibility with the interacting tools. All functions on the Tool Function List should be tested for correctness.

### *17.2 Predictive or Simulation Tools*

To qualify a Simulation Tool, real VHSIC devices should be simulated and the simulated devices should be built in the VHSIC environment being Qualified. The observed behavior of the verifying devices should not be statistically different from its simulated behavior or the difference between simulated and observed behavior should be below the Industry norm for the VHSIC environment. If Industry norms are used to judge the differences between simulated and observed behavior, then the norms should be documented before Qualifying sessions are started.

### *17.3 Design Rules Checkers*

Design Rules Checkers are software systems designed to audit the description of the circuit against a set of prescribed rules. On tools that are rules checkers, test cases should be available to prove that the tool is correctly rejecting those designs that deviate from the rules and accepting those designs that are within the rules. All rules should be verified.

### *17.4 Routing Systems*

A Routing System is a software tool that makes the physical electrical connections between the primitive elements of a VHSIC design placed in the Silicon matrix usually to some design criterion. The automatic routing system should cover at least 99% of the design. The automatic routing system should have some method of specifying and handling critical paths. If the routing system handles multi-metal technologies, then power and ground paths should be restrictable to a single metal level. An interactive router should exist to provide special manual intervention to customize portions of the automatic routers output. The output of the automatic and interactive routers should be comparable. The interactive router should be able to read and manipulate the data base of the automatic router. A net-list or connectivity check should be available to show that the router system has completed its functions while maintaining the original connectivity of the specified circuit. A test should exist to show that the electrical(shorts and opens) and logic functions of the original specified circuit have not been violated. A test should exist to show that the design rules for the mask producing methodology have not been violated.

### *17.5 Mask Generators*

A Mask Generator is a software tool that produces a file of commands that drives equipment to produce the mask set for the VHSIC device given some geometric description of the VHSIC device. For Mask Generators, an extractor should exist that extracts a net-list from the geometry produced by the Generator to show that proper connectivity has been established. A test should exist to show that the electrical(shorts and opens) and logic functions of the original specified circuit have not been violated. Some method should exist to show that the Generator does not violate the mask producing methodology rules.

### *17.6 Silicon Compilers*

A Silicon Compiler is a software tool that produces a file of commands that drives equipment to produce the mask set for the VHSIC device given some higher language description of the VHSIC device. Silicon Compilers should produce output that is within the design rules for the production environment it is used in and its output is expected to pass the Design Rules Checker for the production environment. An extractor should exist to reformat the output of the Silicon Compiler to prove that the



Silicon Compiler did produce the circuit that was entered; functionally, logically and electrically (no shorts or opens). Some method should exist to show that the Compiler does not violate the mask producing methodology rules for the VHSIC environment being Qualified.

### *17.7 Other Tools*

Tools not specifically discussed in the section should be qualified in the following generic manner:

1. The *Tool Function List* should be examined against the *Tool Qualifying Plan* to insure that all functions are included in the plan.
2. The *Tool Dependency List* should be examined against the *Tool Qualifying Plan* to insure that all tool communication dependencies are tested.
3. The *Tool Qualifying Plan* should be examined for completeness, reasonableness and is within Industry norms for the Tool type and VHSIC environment.
4. The Journaling and Playback functions should be tested against Documentation.
5. All Permanent Files should be tested against documented format requirements.